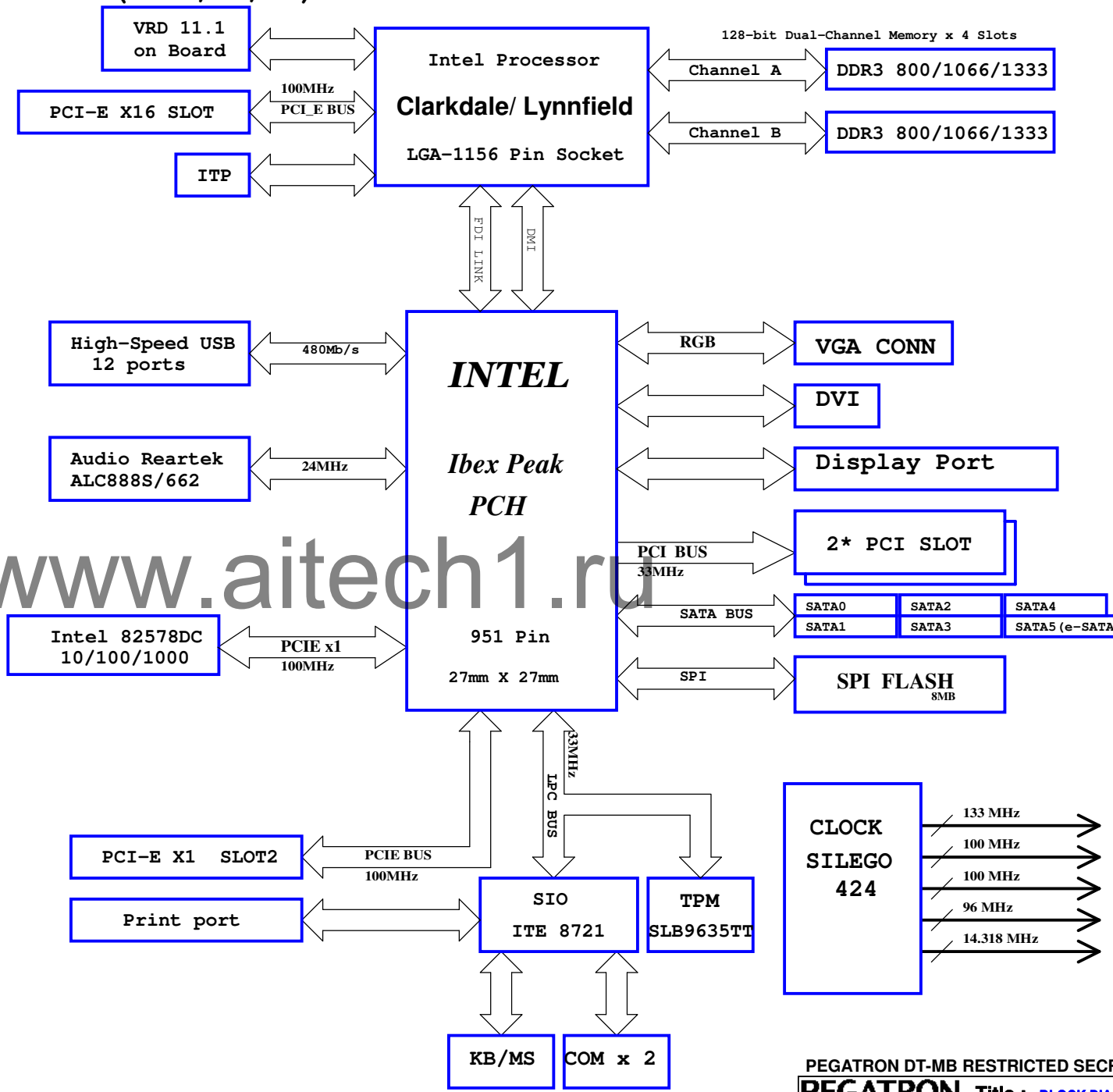
POS-PIQ57BQ

Revision: R1.01 (2010/04/20)

PAGE	TITLE
01	BLOCK DIAGRAM
02	CHANGE HISTORY
03	CLOCKS DISTRIBUTION
04	SIGNAL & RESET MAP
05	POWER FLOW
06	POWER DISTRIBUTION
07	POWER SEQUENCE
08	CLOCK SLG8SP424
09	VID RESISTER
10~15	CPU_SOCKET1160_MEMORY 1 - 6
16	DDR3 CHANNEL A
17	DDR3 CHANNEL B
18	DDR3 TERMINATION A&B
19	PCI EXPRESS X 16 SLOT
20~28	INTEL PCH 1 - 9
29	INTEGRATED VGA PORT
30	DVI LEVEL SHIFTER
31	DVI CONTROL
32	DVI-I CONNECTOR
33	Intel 82578DC LAN
34	RJ45+USB CONNECTER
35	Dual USB CONNECTER
36	PCI EXPRESS X1 SLOT -1
37	PCI SLOT INTERFACE - PCI-1
38	PCI SLOT INTERFACE - PCI-2
39	RTL 888S/662 AZALIA CODEC
40	FRONT AUDIO CONNECTOR
41	Azalia Rear Audio Connector
42	USB HEADER CONNECTOR - 1
43	USB HEADER CONNECTOR - 2
44	SATA & TPM CONNECTOR
45	SPI SERIAL FLASH & SMBUS
46	SUPER I/O - ITE 8721-1
47	SUPER I/O - ITE 8721-2
48	FAN CIRCUIT FOR 4 - PIN
49	FRONT PANEL CIRCUIT FOR CPC
50	RTC / CMOS / SCREW/KM
51	RSMRST CIRCUIT / EMI
52	CPU ITP / LPC DEBUG CONN
53	RTL8111DL LAN
54	LED / COM / SPKR / INTRUDER
55	LPT
56	ATX POWER CONNECTOR
57	VCORE CONTROLLER
58	VCORE DRIVER1
59	VCORE DRIVER2
60	VAGX CONTROLLER
61	VAGX DRIVER
62	+1P1V_VTT
63	+1P5V_DUAL
64	+1P05V_PCH / +1P05V_ME
65	+5V_DUAL / +3P3V_ME
66	+SM_VTT / +1P8V_SFR



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : BLOCK DIAGRAM

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Friday, April 23, 2010 Sheet 1 of 68

Schematics Change History

Version	Date	Comments
1.01	2010/03/23	1.Change PCE20,PCE21BOM to 11X090567160. SR92 BOM to 10X212100510.
1.01	2010/03/23	2.SIO pin 76 pull high to +5VSB_ATX form ITE vender request.(Fix EuP mode issue)
1.01	2010/03/23	3.Remove +3P3V_ME schematic to meet core team request.
1.01	2010/03/23	4.Change VC10,VC11,VC12,VC13 BOM default NI.10X212300040
1.01	2010/03/23	5.Change VR8 , VR9 to 10X212300040
1.01	2010/03/24	
1.01	2010/03/24	7.Change P1R4 to 10X212100140 , Del P1R1 , ADD O2R28.
1.01	2010/03/24	8.D3CB7,D3CB15 from 0.1uF to 2.2uF,to fix EA VREF_CA issue
1.01	2010/03/25	9 . O3Q1' O3R2'O3R10 to NI.Change O3R6'O3Q2'O3R11 to I.
1.01	2010/03/29	10.Change [VL2,4,6 change to 0 ohm]_[VL3,5,7 to 0.068UH/300mA]_[VC1,4,7 default NI]to fix EA VGA signal issue.
1.01	2010/03/29	
1.01	2010/03/29	12.SR83,SR88 from 33 ohm to 22 ohm,to Fix VGA EA issue.
1.01	2010/03/30	13.Add HR60,to fix EA RESET signal issue.
1.01	2010/04/01	14.Change +1P5V_DUAL_OV to SIO GP10.
1.01	2010/04/02	13.Add M1C15 , M1C18 for DP.

CAD Note:

Default component footprint is SMD 0402, Y5V, 5% type. Difference footprint show on schematics.

Property: BOM

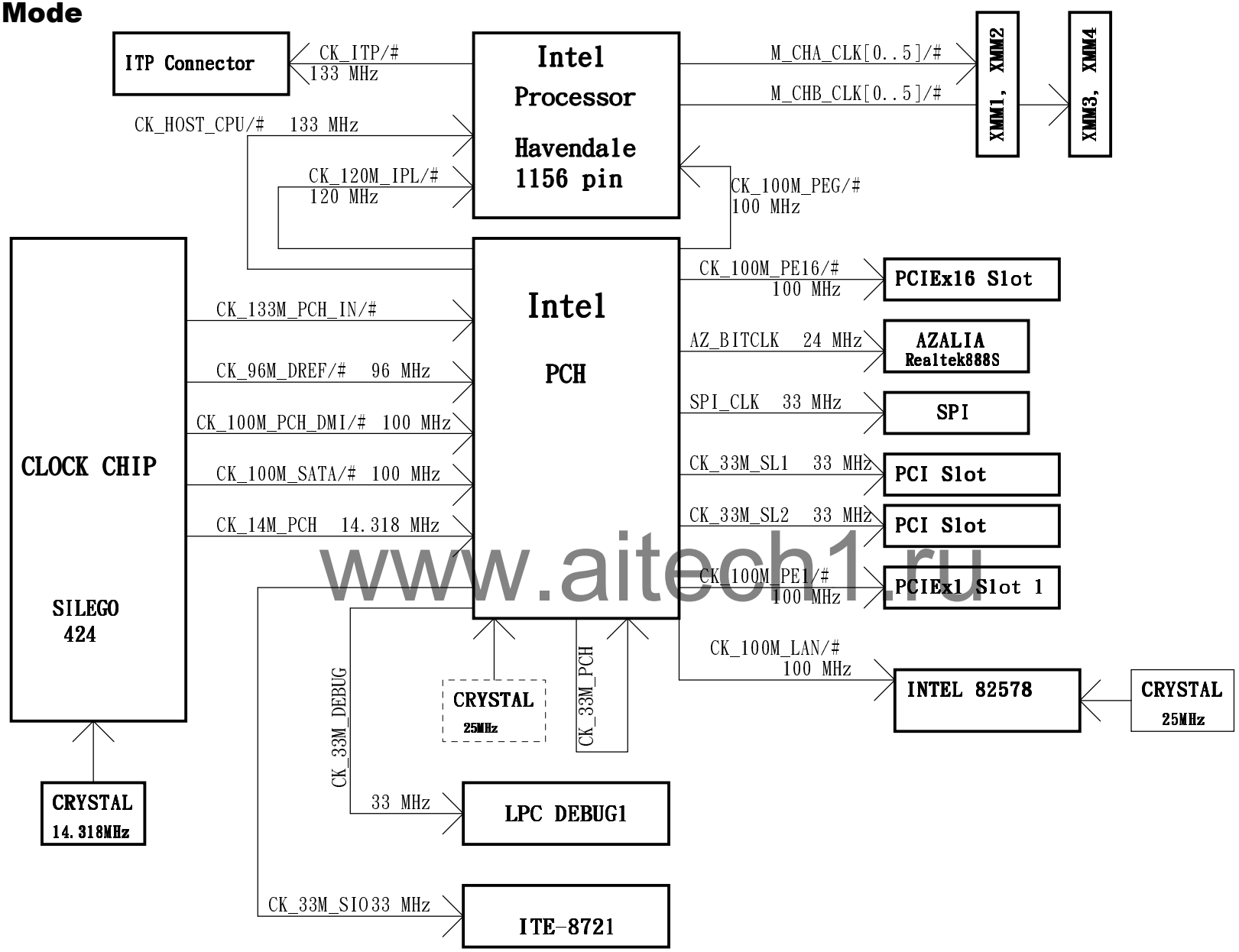
I = Installed Part.

NI = Not Installed Part.

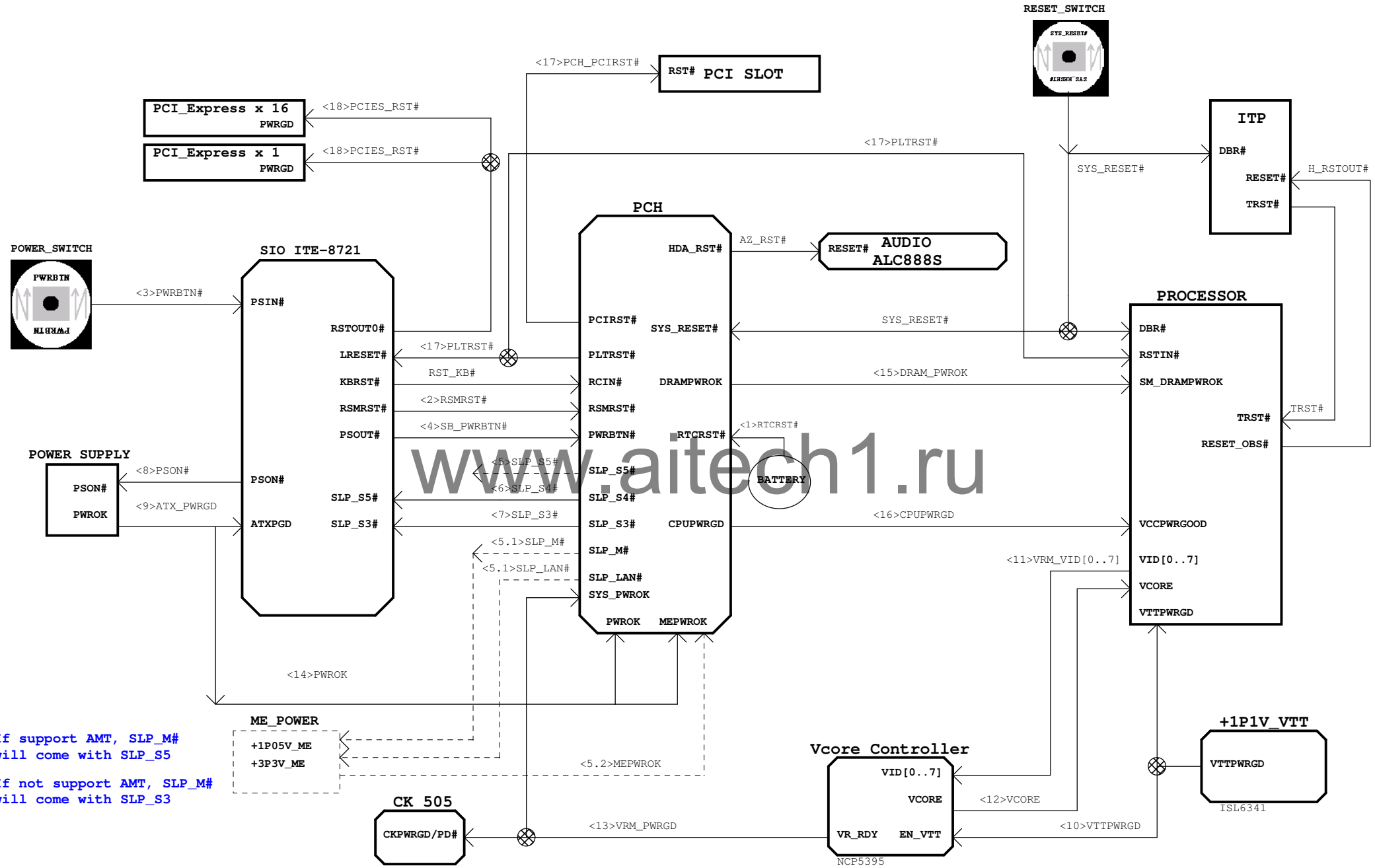
PROTO = PROTO Phase Only.

VP = Virtual Part.

PCH Buffer Mode



PEGATRON	Title : CLOCK DISTRIBUTION	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Tuesday, March 23, 2010	Sheet 3 of 68	

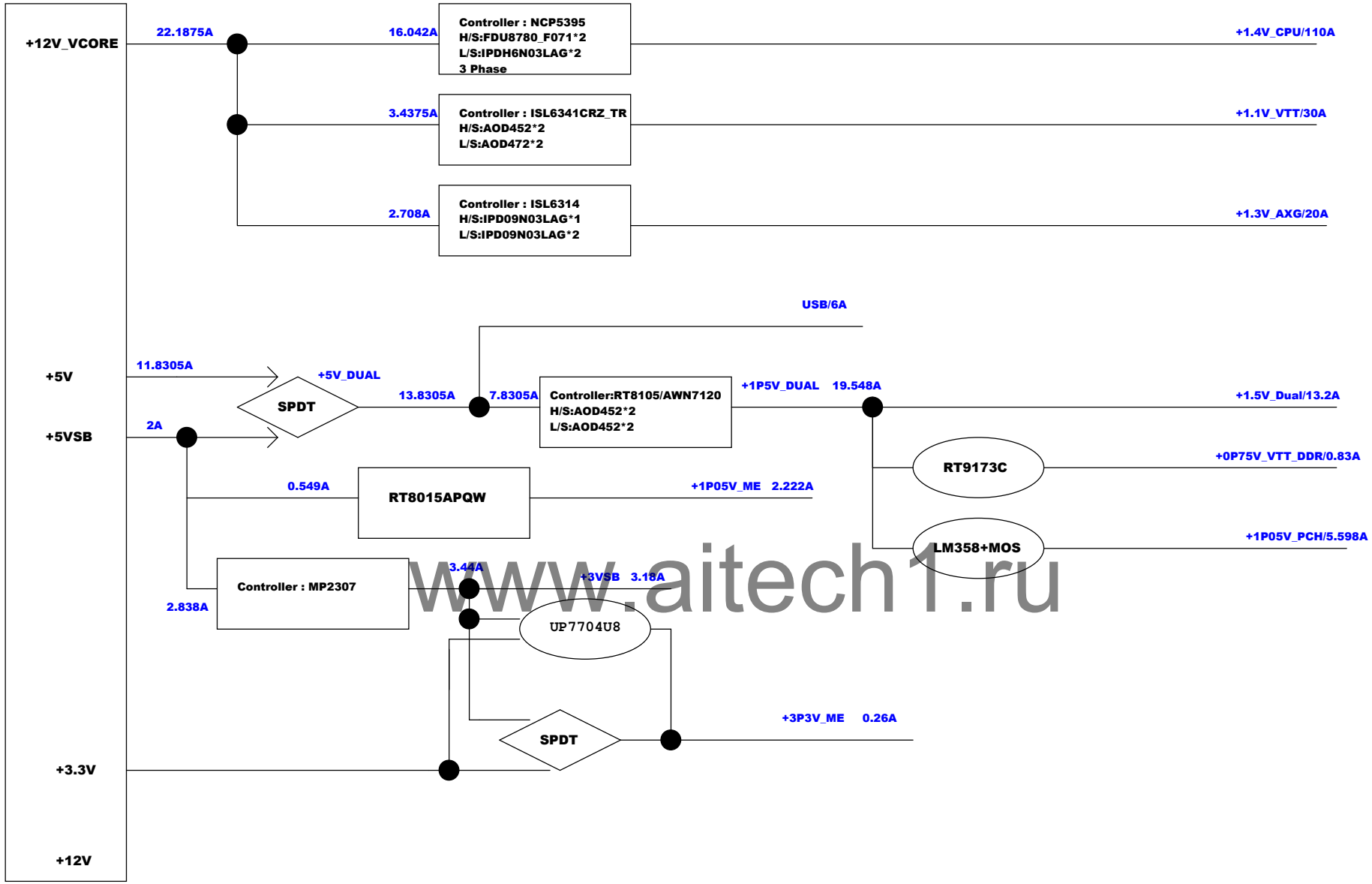


PEGATRON Title : SIGNAL & RESET MAP

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Tuesday, March 23, 2010 Sheet 4 of 68



SWITCHING LINEAR SWITCH ON/OFF

<Variant Name>

PEGATRON Title : POWER FLOW

PEGATRON CORPOATION Engineer: Michael Lee

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Tuesday, March 23, 2010 Sheet 5 of 68

Lynnfield/Clarkdale

VCORE
+1.1V_VTT
+1.5V
+1.8V

-> 90A - 95(TBD)W
-> 30A(TBD) - 33W
Vddq -> 6A - 9W
Vccpll -> 1.35A - 2.43W

Intel Ibex Peak

V_CPU_IO
+5V
+5V
+3.3V
+1.1V
+1.05V
+1.8V
+3P3V
+3P3VSB

-> <1mA - 1.1mW
V5REF -> <1mA - 5mW
V5REF_Sus -> <1mA - 5mW
Vcc3_3 -> 0.357A - 1.178W
VccDAC -> 0.069A - 0.228W
VccDMI -> 0.065A - 0.07W
VccADPLLA -> 0.075A - 0.079W
VccADPLLB-> 0.075A - 0.079W
VccCORE -> 1.629A - 1.71W
VccIO -> 3.251A - 3.414W
VccLAN -> 0.372A - 0.39W
VccME -> 2.222A - 2.333W
VccqNAND -> 0.156A - 0.281W
VccVRM -> 0.196A - 0.353W
VccTX_LVDS -> 0.059A - 0.106W
VccALVDS -> <1mA - 3.3mW
VccRTC -> 2mA - 6.6mW
VccSus3_3 -> 0.168A - 0.554W
VccSusHDA -> 0.006A - 0.02W
VccME3_3-> 0.086A - 0.284W

CLOCK- CK505

+3P3V
+VDD_IO (0.8V)

-> 250mA - 0.825W
-> 80mA - 64mW

DDR3 DIMM (4) & Termination

+1.5V_DAUL
SM_VTT(0.75V)

VDD (SO, S1) -> 7.2 A - 10.8W
VDD (S3) -> 712mA - 1.07W
SM VTT (SO, S1) -> 0.83A - 0.623W

PCI Express x 1

+12V
+3P3V
+3P3V_PCI

-> 0.5A - 6W
-> 3.0A - 9.9W
WAKE -> 0.375A - 1.24W
No WAKE-> 20mA - 66mW

PCI Express x 16

+12V
+3P3V
+3P3V_PCI

-> 5.5A - 66W
-> 3.0A - 9.9W
WAKE -> 0.375A - 1.24W
No WAKE-> 20mA - 66mW

PCI SLOTS

+12V
-12V
+5V
+3P3V
+3P3V_PCI

-> 0.5A - 6W
-> 0.1A - 1.2W
-> 5.0A - 25W
-> 7.6A - 25.08W
WAKE -> 0.375A - 1.24W
No WAKE-> 20mA - 66mW

INTEL 82578

+3P3V_CL
+1P8VSB_LAN
VCC_LAN(1.05V)

-> 15.3mA(TBD) - 31.15mW
-> 300mA - 540mW
-> 300mA -315mW

SIO ITE-8721

+5V
+3.3VSB
+3.3V

-> 1mA - 5mW
-> 2.4uA - 7.92uW
-> 2mA - 6.6mW

ALC888S Azalia Codec

+5VSB
+3P3V

-> 0.6A - 3W
-> 0.4A - 1.32W

USB 12 PORTS

+5V_DUAL

(SO, S1) -> 8.4A - 42W
(S3) -> 0.336A - 1.68W

1394A

+3P3V

-> mA - W

HDMI

+3P3V
+2P5V_DVI

-> mA - mW
-> mA - mW

SATA 6 PORTS

+5V
+12V

-> 0.975A - 4.875W
-> 0.9A - 10.8W

FAN

+12V

-> 0.6A - 7.2W

PS2 KB/MS

+5V_DUAL

(SO, S1) -> 0.345A - 1.73W
(S3) -> 2mA - 10mW

SPI

+3V

-> 30mA - 99mW

HDD

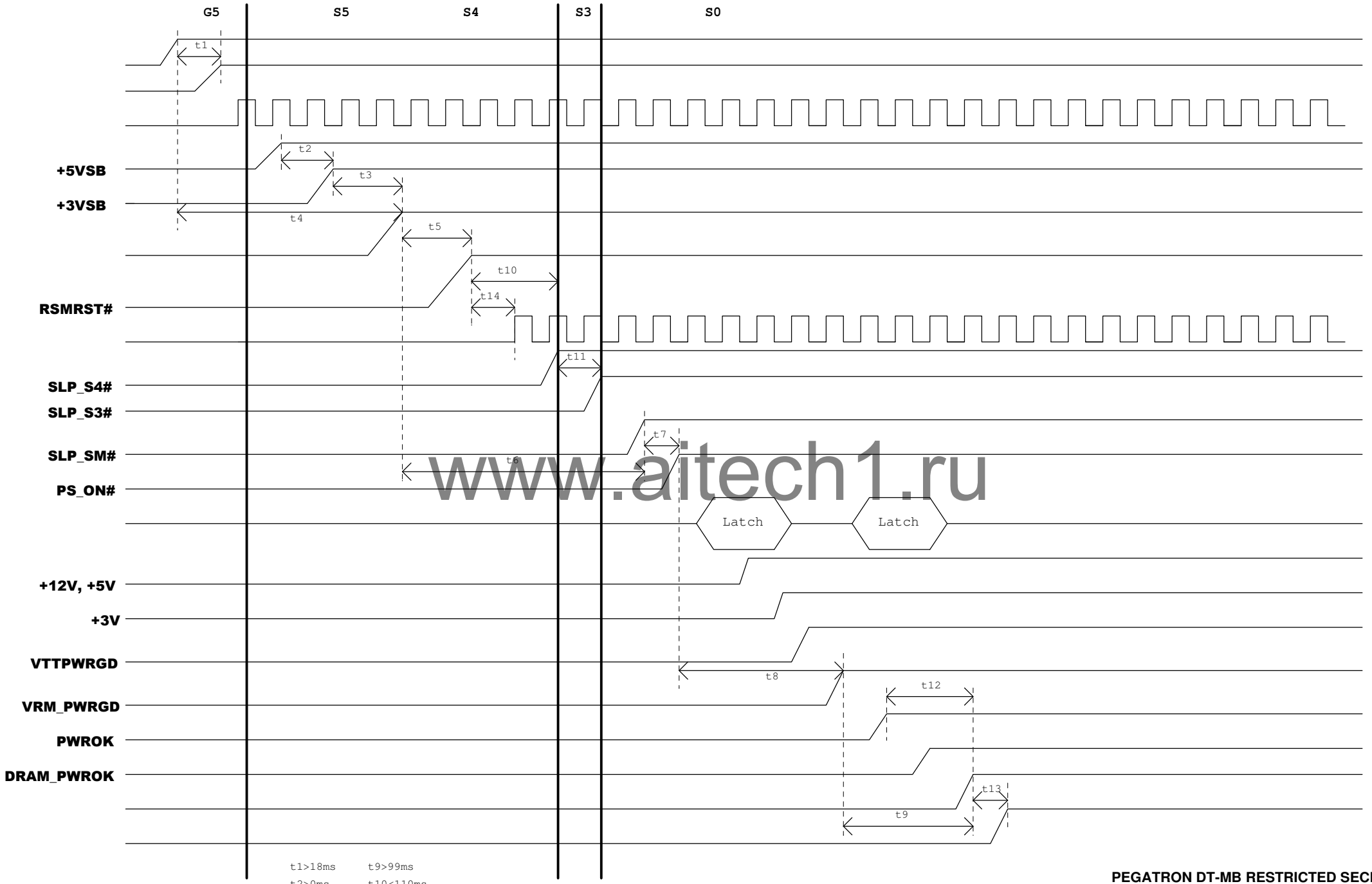
+12V
+5V

-> 0.75A - 9.0W
-> 0.75A - 3.75W

CD ROM

+12V
+5V

-> 0.75A - 9.0W
-> 0.75A - 3.75W



The data is not final

t1>18ms
t2>0ms
t4>0ms
t5>10ms
t6>0ms
t7>0ms
t9>99ms
t10<110ms
t11>1RTCCLK
t12>5ms
t13:35~74RTCCLK
t14<110ms

PEGATRON DT-MB RESTRICTED SECRET

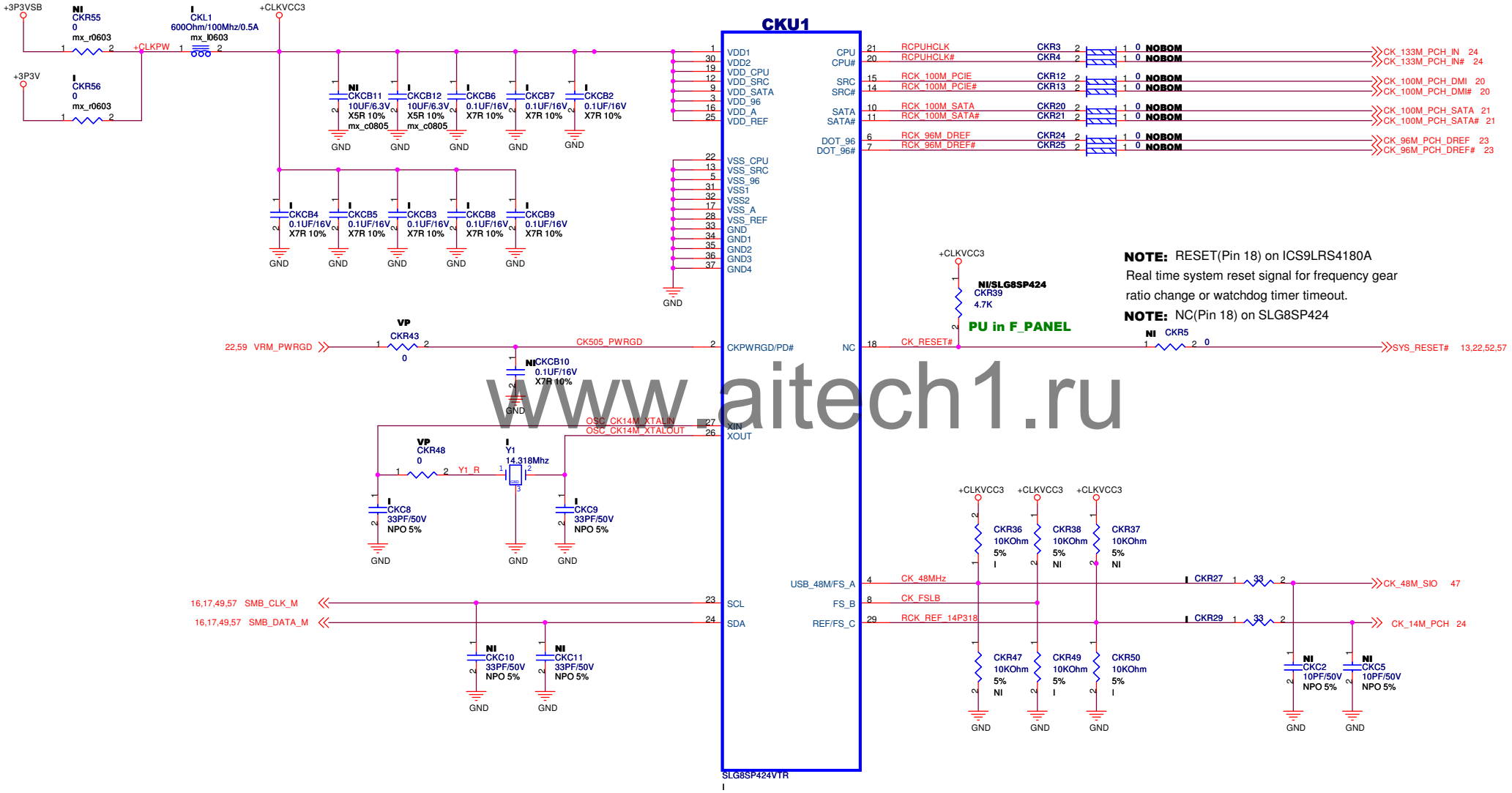
PEGATRON Title : POWER SEQUENCE

Pegatron Corp. Engineer: Michael Lee

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Tuesday, March 23, 2010 Sheet 7 of 68

ICS9LRS4180AKLFT: 0610-0038000
SLG8SP424VTR: 0610-007D000



NOTE: RESET(Pin 18) on ICS9LRS4180A
Real time system reset signal for frequency gear ratio change or watchdog timer timeout.

NOTE: NC(Pin 18) on SLG8SP424

NOTE:

FSLC	FSLB	FSLA	CPU FREQ
0	0	1	133MHz
1	0	1	100MHz

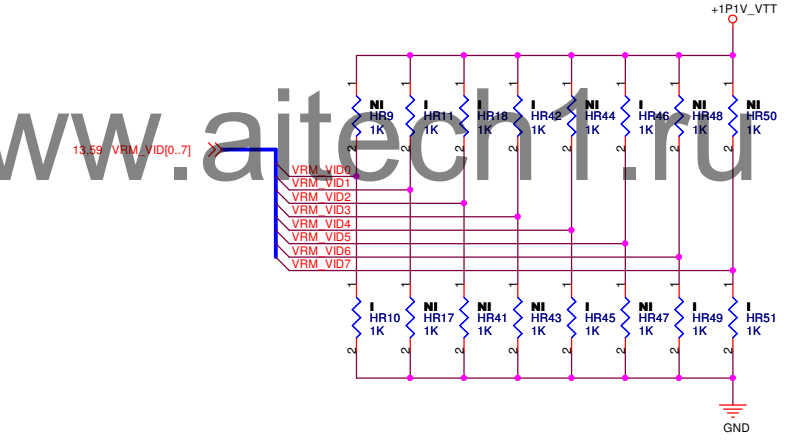
PEGATRON DT-MB RESTRICTED SECRET

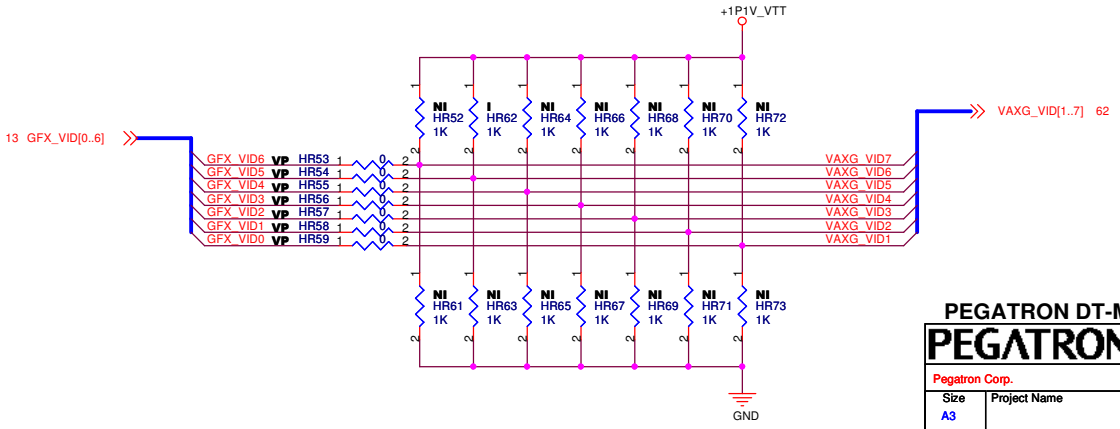
PEGATRON Title : ICS 4180/SLG 424

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 8 of 68





POWER ON CONFIGURATION (POC) TABLE

	FUNCTION	DEFAULT
VID0	MSI0	0
VID1	MSI1	1
VID2	MSI2	1
VID3	IMON CONFIG0	1
VID4	IMON CONFIG1	0
VID5	IMON CONFIG3	1
VID6	RESERVED	
VID7	VRD SELECT	LOW
PSI#	RESERVED	LOW

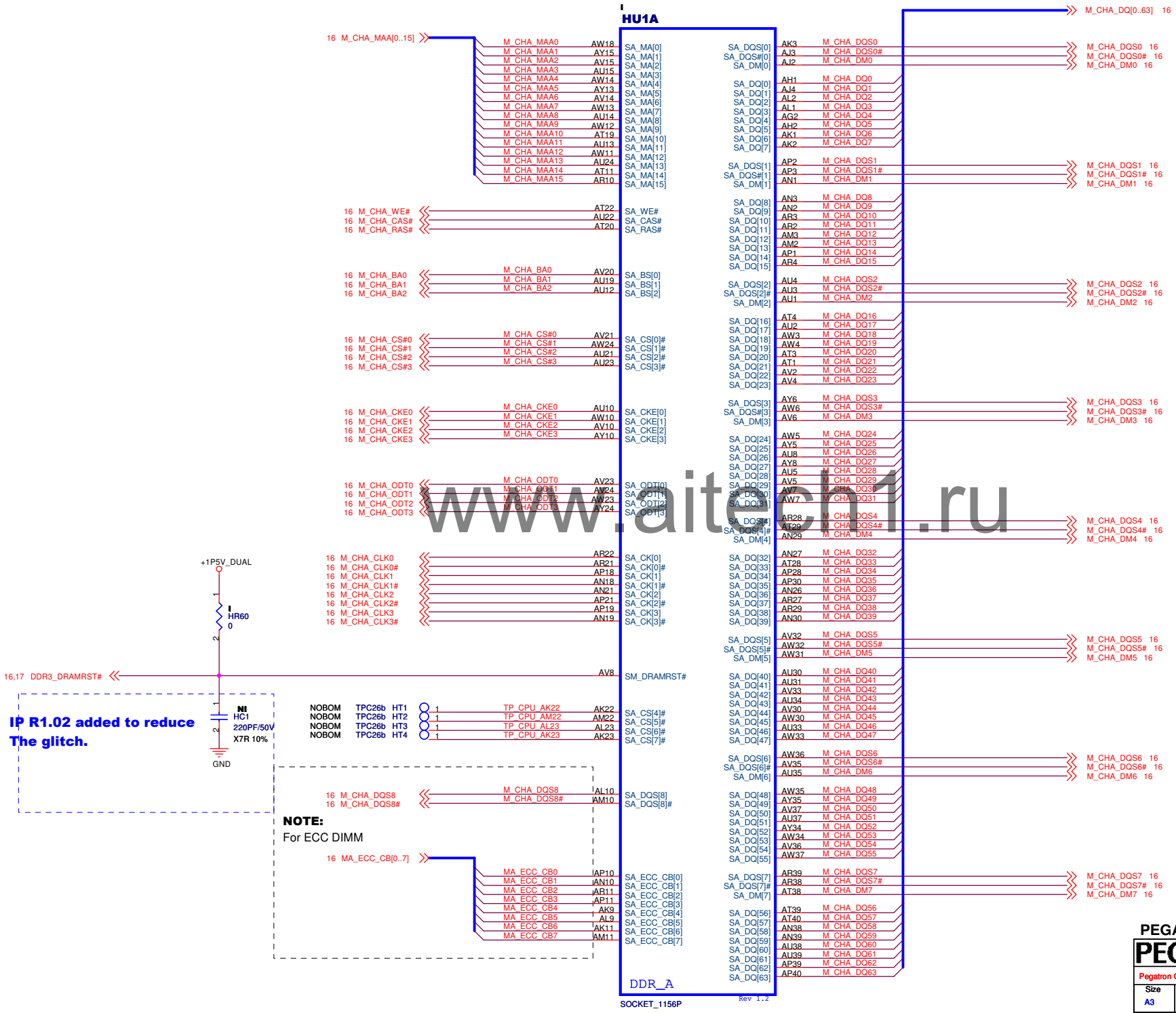
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VID RES

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 9 of 68



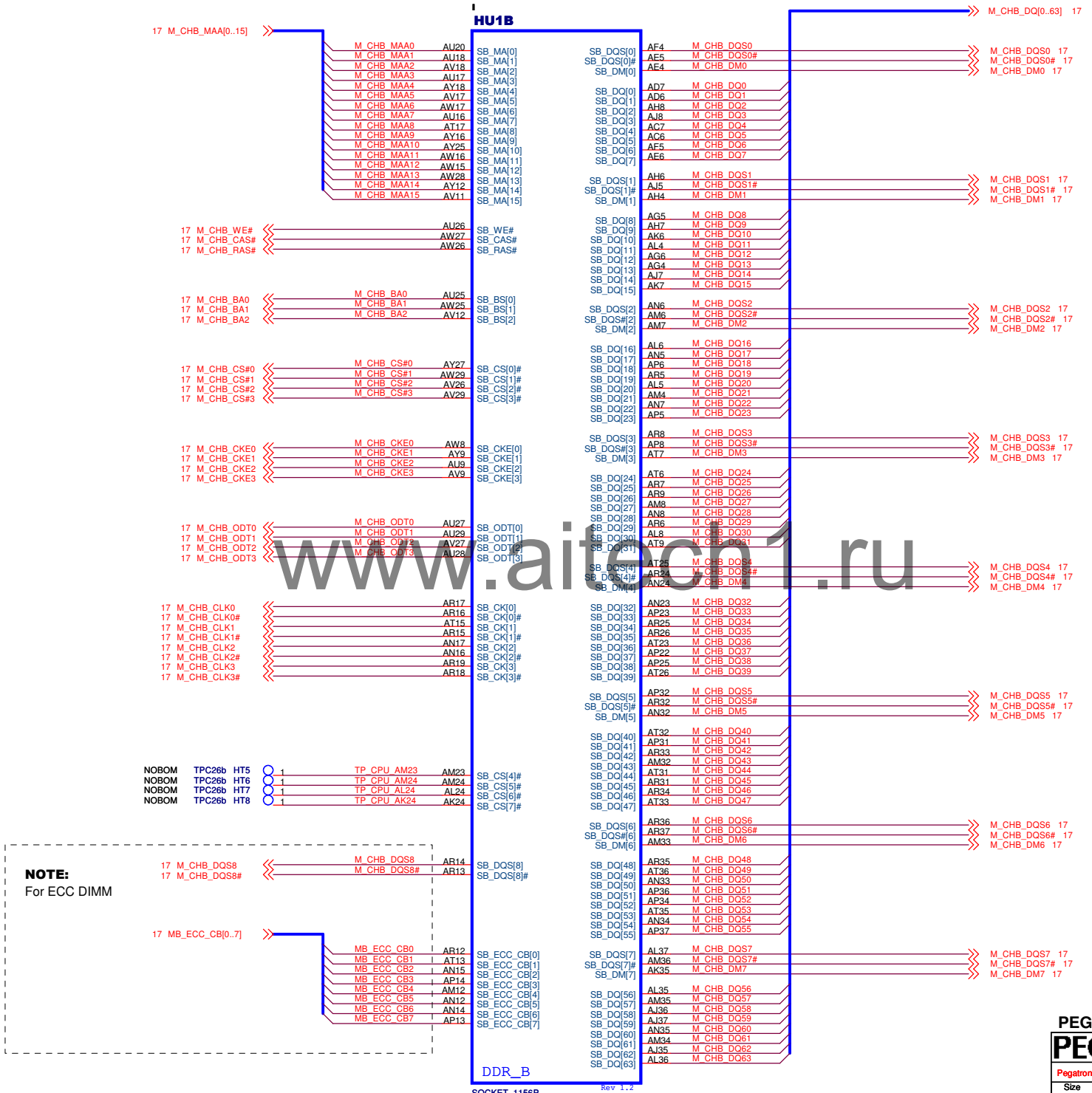
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU 1160 + MEMORY - 1

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 10 of 68



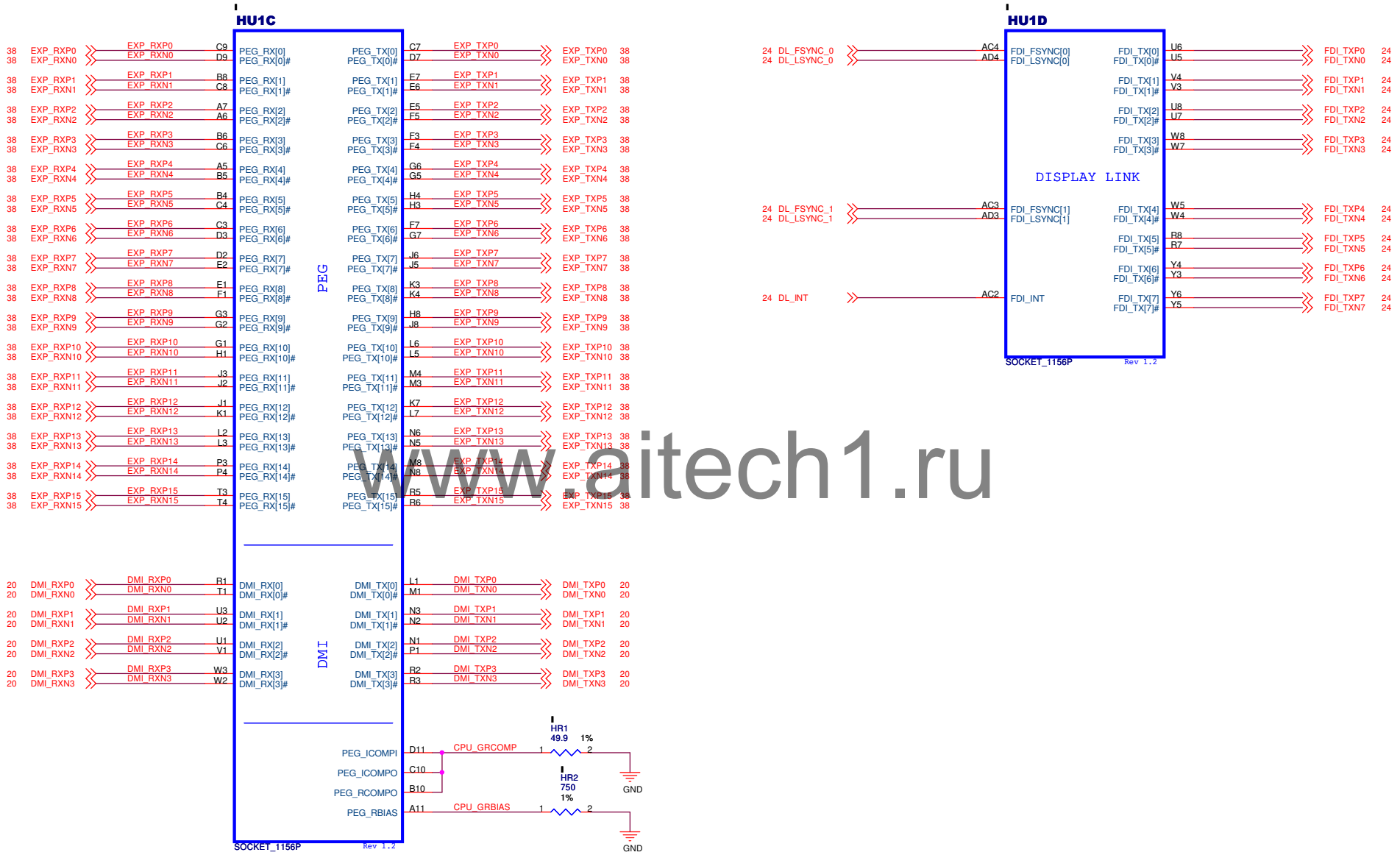
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU 1160 + MEMORY - 2

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 11 of 68



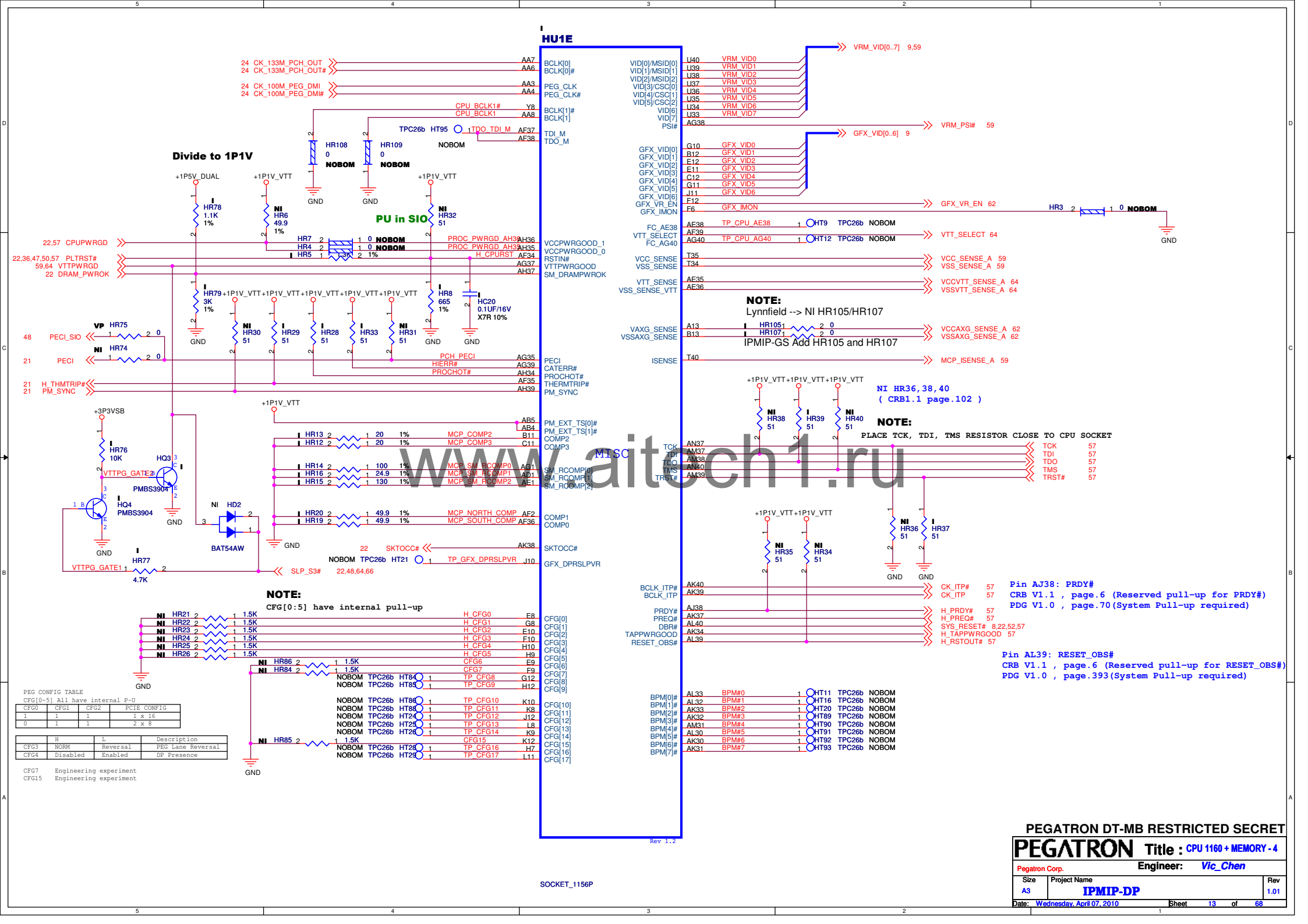
PEGATRON DT-MB RESTRICTED SECRET

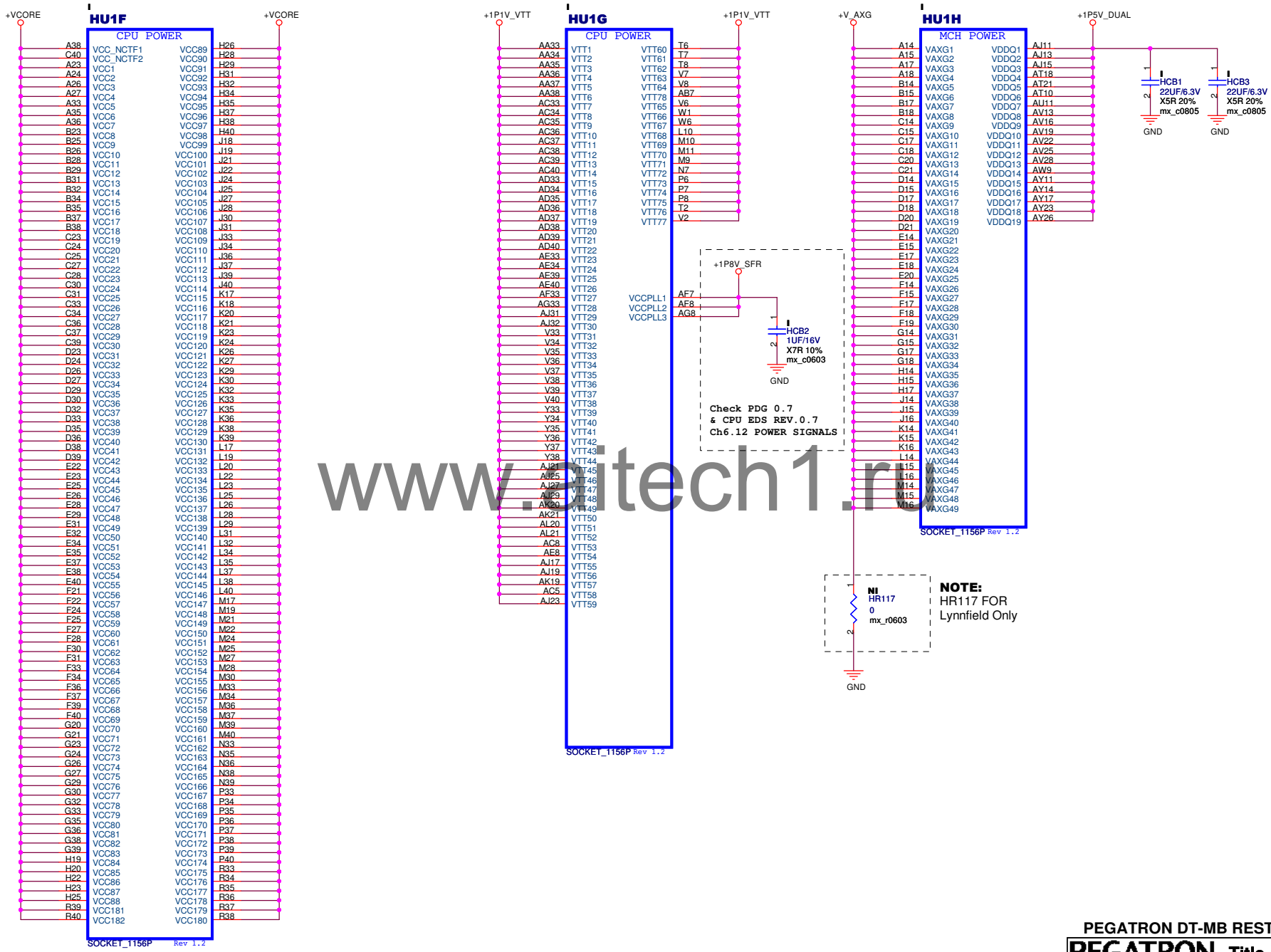
PEGATRON Title : CPU 1160 + MEMORY - 3

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 12 of 68





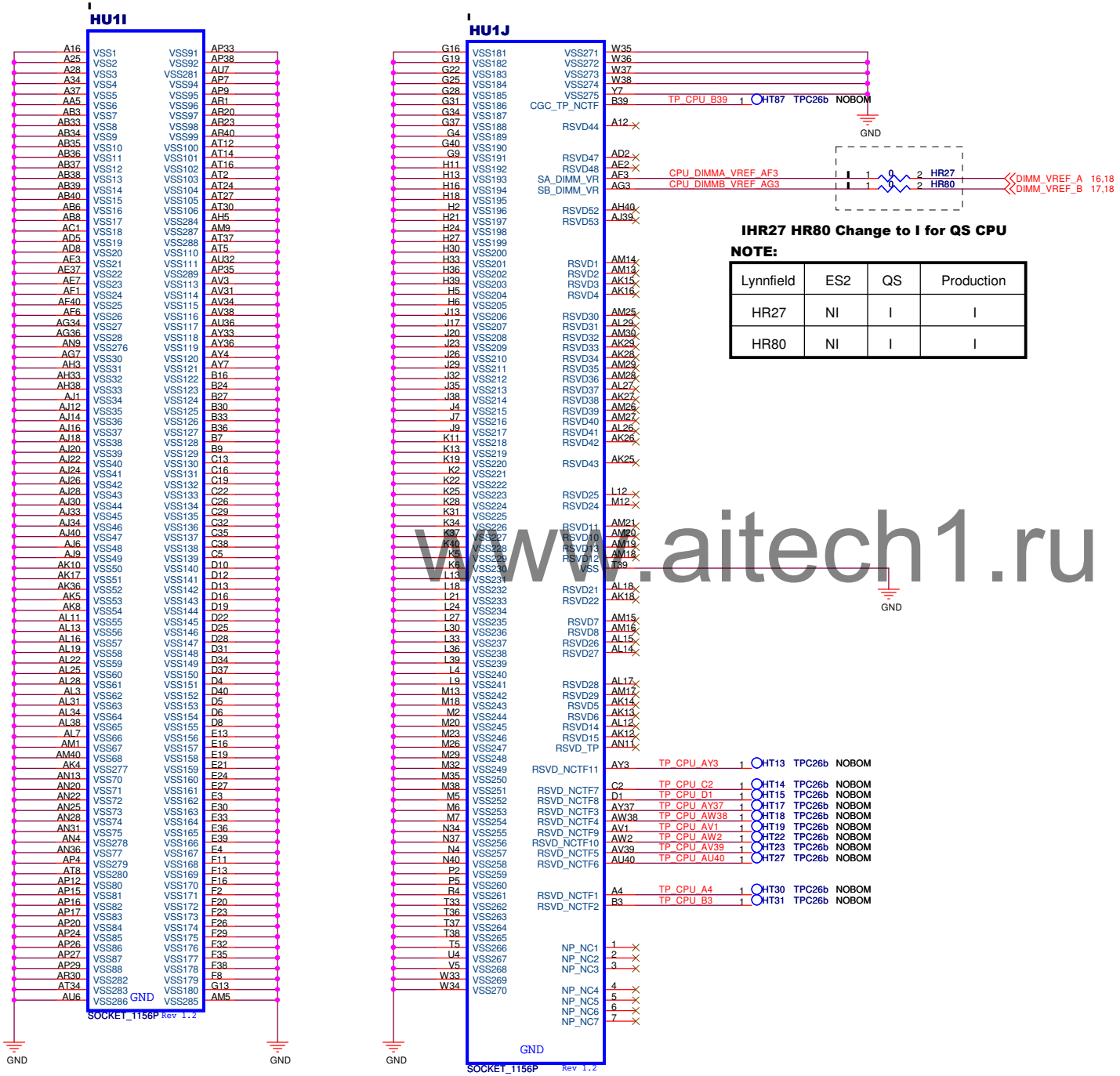
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU 1160 + MEMORY - 5

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Tuesday, March 23, 2010 Sheet 14 of 68



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : CPU 1160 + MEMORY - 6

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 15 of 68

NOTE:
Below 4 signals are different connection in Eaglelake DDR3 platform
Channel A : CS1/WE/MA0
Channel B : ODT3

XMM1 COLOR: BLUE

XMM2 COLOR: BLACK

XMM1A

XMM2A

XMM1B

XMM2B

NOTE:
Check clock source if CPU implemented

NOTE:
For ECC DIMM

DDR3_DIMM_240P

M_CHA_DQ[0..63] 10
M_CHA_MAA[0..15] 10

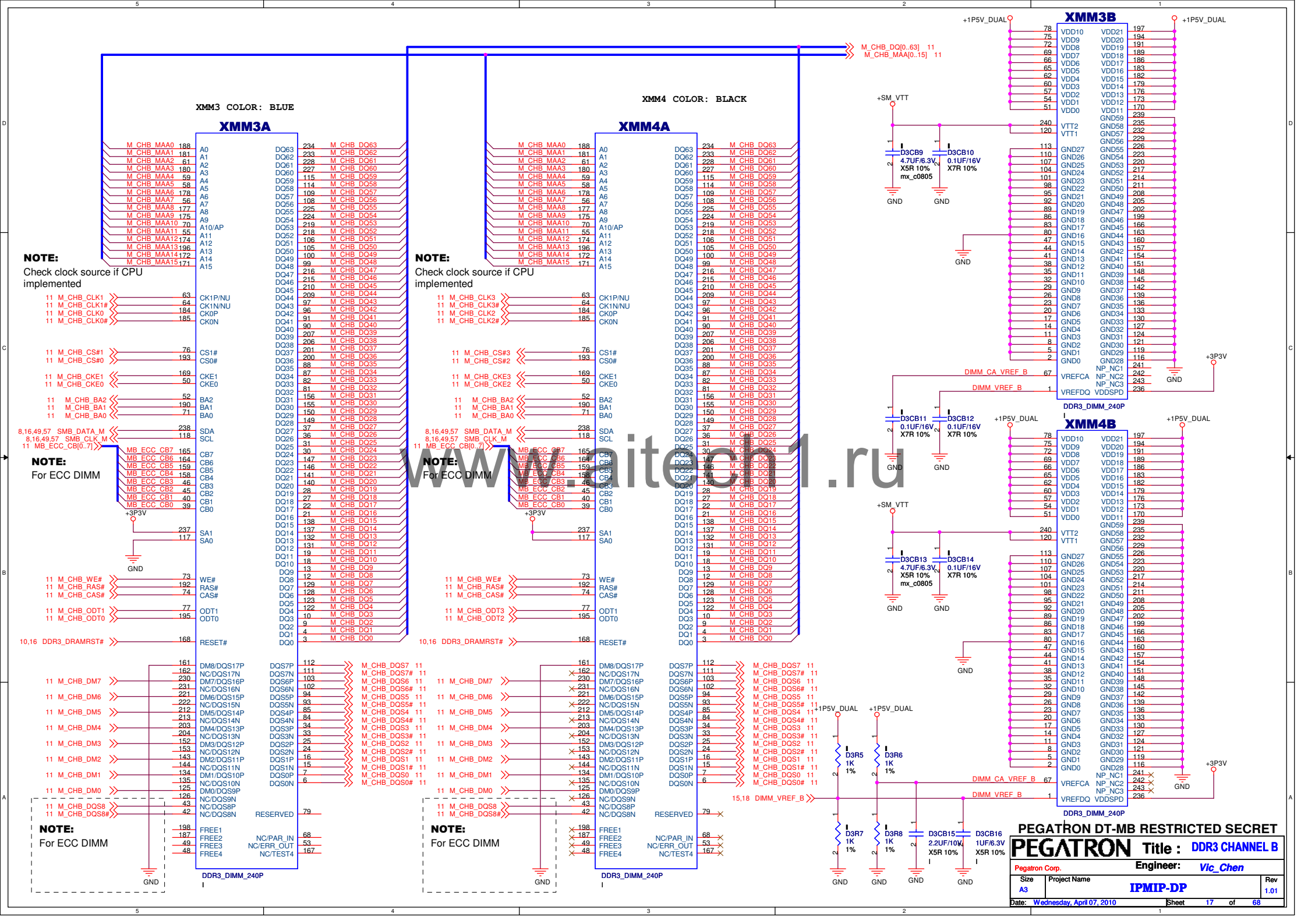
+1P5V_DUAL
+SM_VTT
+3P3V
GND

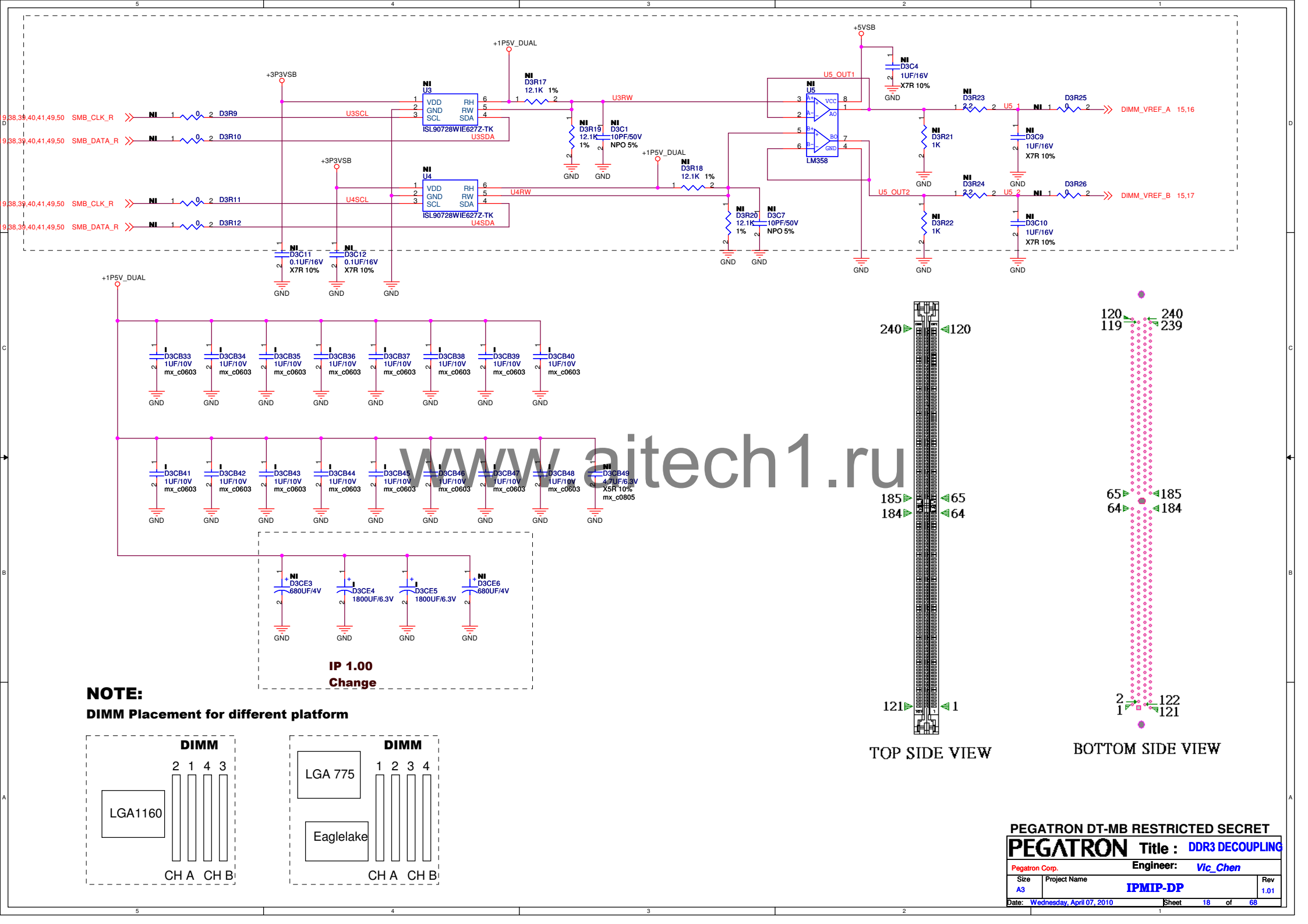
D3CB1 4.7UF/6.3V X5R 10% mx_c0805
D3CB2 0.1UF/16V X7R 10%
D3CB3 0.1UF/16V X7R 10%
D3CB4 0.1UF/16V X7R 10%
D3CB5 4.7UF/6.3V X5R 10% mx_c0805
D3CB6 0.1UF/16V X7R 10%
D3R1 1K 1%
D3R2 1K 1%
D3R3 1K 1%
D3R4 1K 1%
D3CB7 2.2UF/10V X5R 10%
D3CB8 1UF/6.3V X5R 10%

DIMM_CA_VREF_A
DIMM_VREF_A
15,18 DIMM_VREF_A

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title :	DDR3 CHANNEL A
Pegatron Corp.	Engineer:	Vic_Chen
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 16 of 68	





P55 ES2: 0200-006T000

U1A

Strap
(GNT0#~GNT3# have IPU)

GNT3#	0	TOP Block SWAP
	1	Normal(Default)

GNT2#	0	ESI mode (Server Only)
	1	DMI(Default)

GNT1#	GNT0#	BOOT BIOS
1	0	RESERVED
0	1	PCI
1	1	SPI
0	0	LPC

PCI
SMBUS
RTC
SPI
IBEXPEAK Rev 1.0

Strap

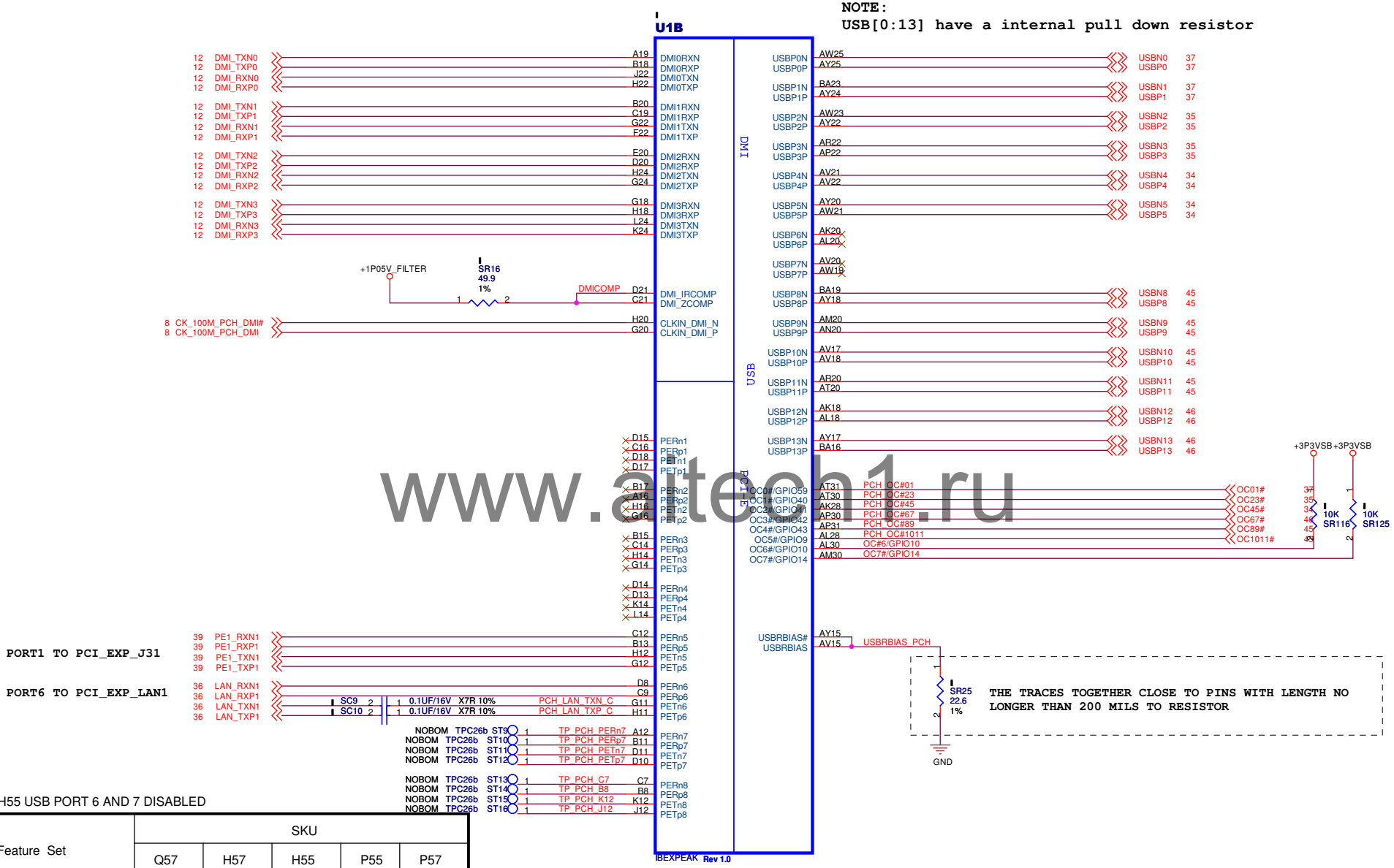
SPI_MOSI (IPD)	0	Disable ITPM (Default)
	1	Enable ITPM

CRB R1.0 (page.39) suggests that don't change it to 0402 package type

XY5
Crystal Holder

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL_PCH-1
Pegatron Corp. Engineer: Vic_Chen
Size A3 | Project Name IPMIP-DP | Rev 1.01
Date: Thursday, April 08, 2010 | Sheet 19 of 68



NOTE: FOR H55 USB PORT 6 AND 7 DISABLED

Feature Set	SKU				
	Q57	H57	H55	P55	P57
PCI Express 2.0	8	8	6	8	8
USB 2.0	14	14	12	14	14
SATA	6	6	6	6	6
HDMI/DVI/VGA/SDVO/DisplayPort	YES	YES	YES	NO	NO

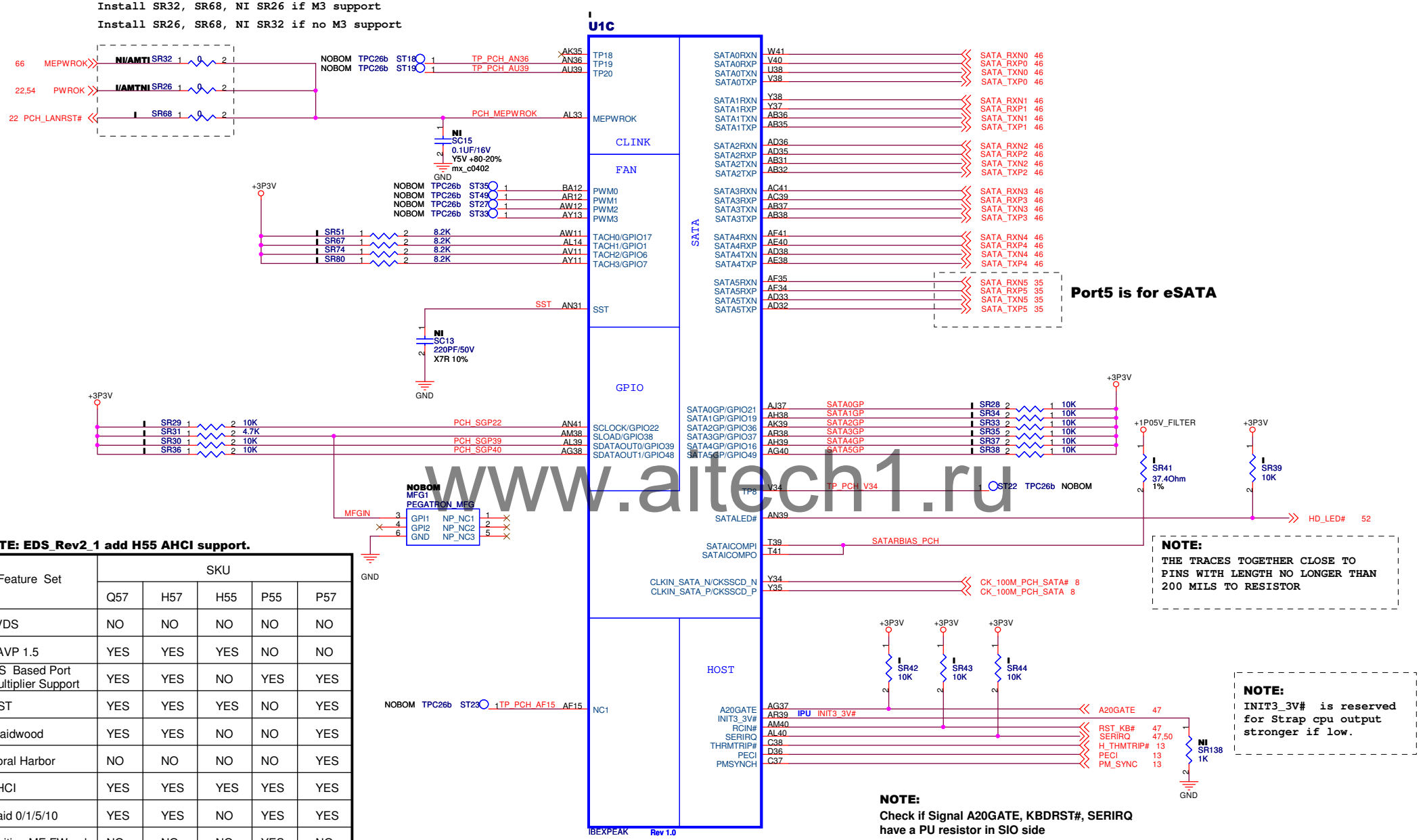
PEGATRON Title : INTEL_PCH - 2

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 20 of 68

NOTE:
Install SR32, SR68, NI SR26 if M3 support
Install SR26, SR68, NI SR32 if no M3 support



NOTE: EDS_Rev2_1 add H55 AHCI support.

Feature Set	SKU				
	Q57	H57	H55	P55	P57
LVDS	NO	NO	NO	NO	NO
PAVP 1.5	YES	YES	YES	NO	NO
FIS Based Port Multiplier Support	YES	YES	NO	YES	YES
QST	YES	YES	YES	NO	YES
Braidwood	YES	YES	NO	NO	YES
Coral Harbor	NO	NO	NO	NO	YES
AHCI	YES	YES	YES	YES	YES
Raid 0/1/5/10	YES	YES	NO	YES	YES
Ignition ME FW only	NO	NO	NO	YES	NO
AT-p	YES	NO	NO	NO	NO
iAMT 6.0	YES	NO	NO	NO	NO
IRPA for Business	YES	NO	NO	NO	NO
IRPA for Consumer	NO	YES	NO	NO	NO
IRWT	NO	YES	YES	NO	NO

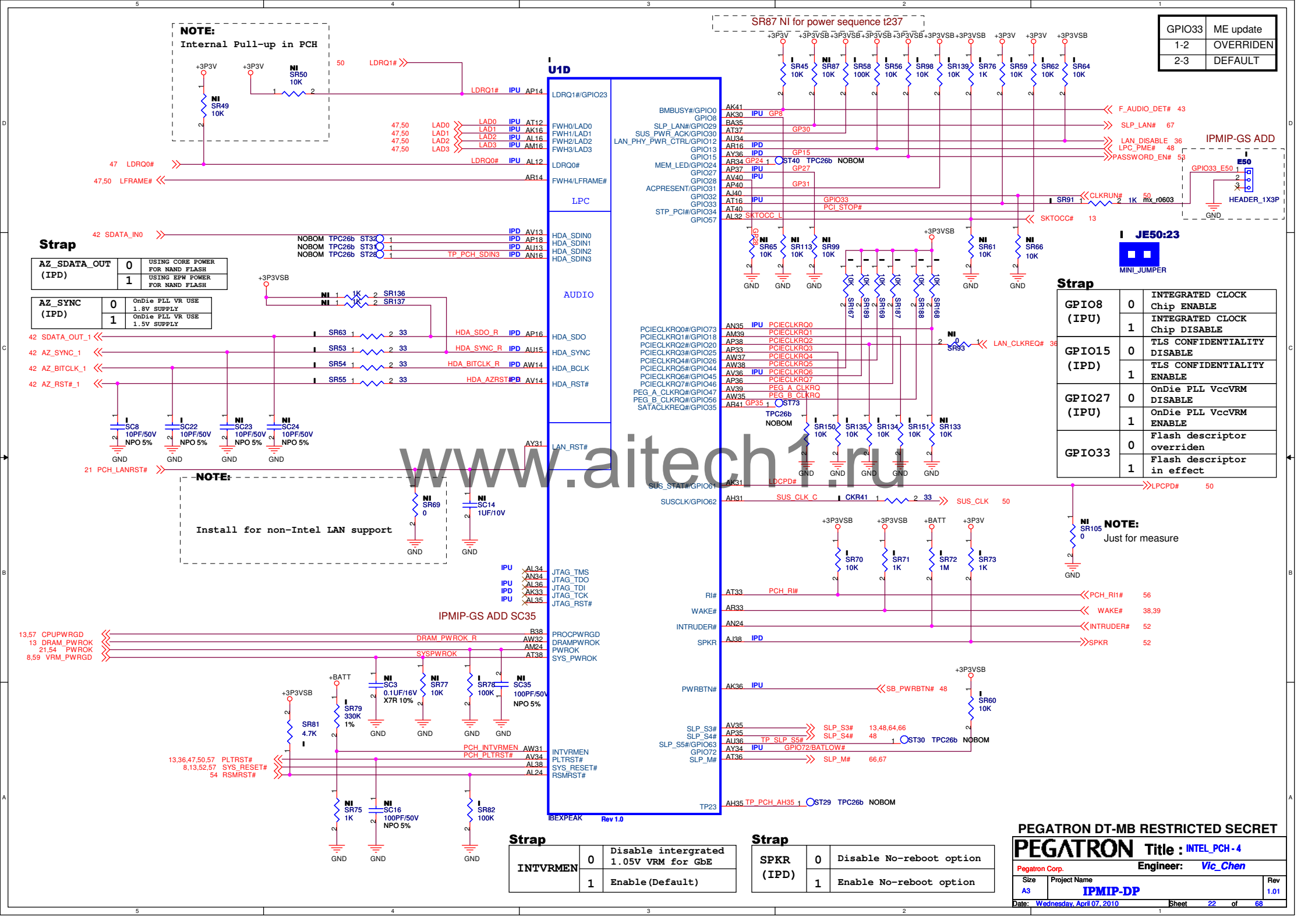
PEGATRON DT-MB RESTRICTED SECRET

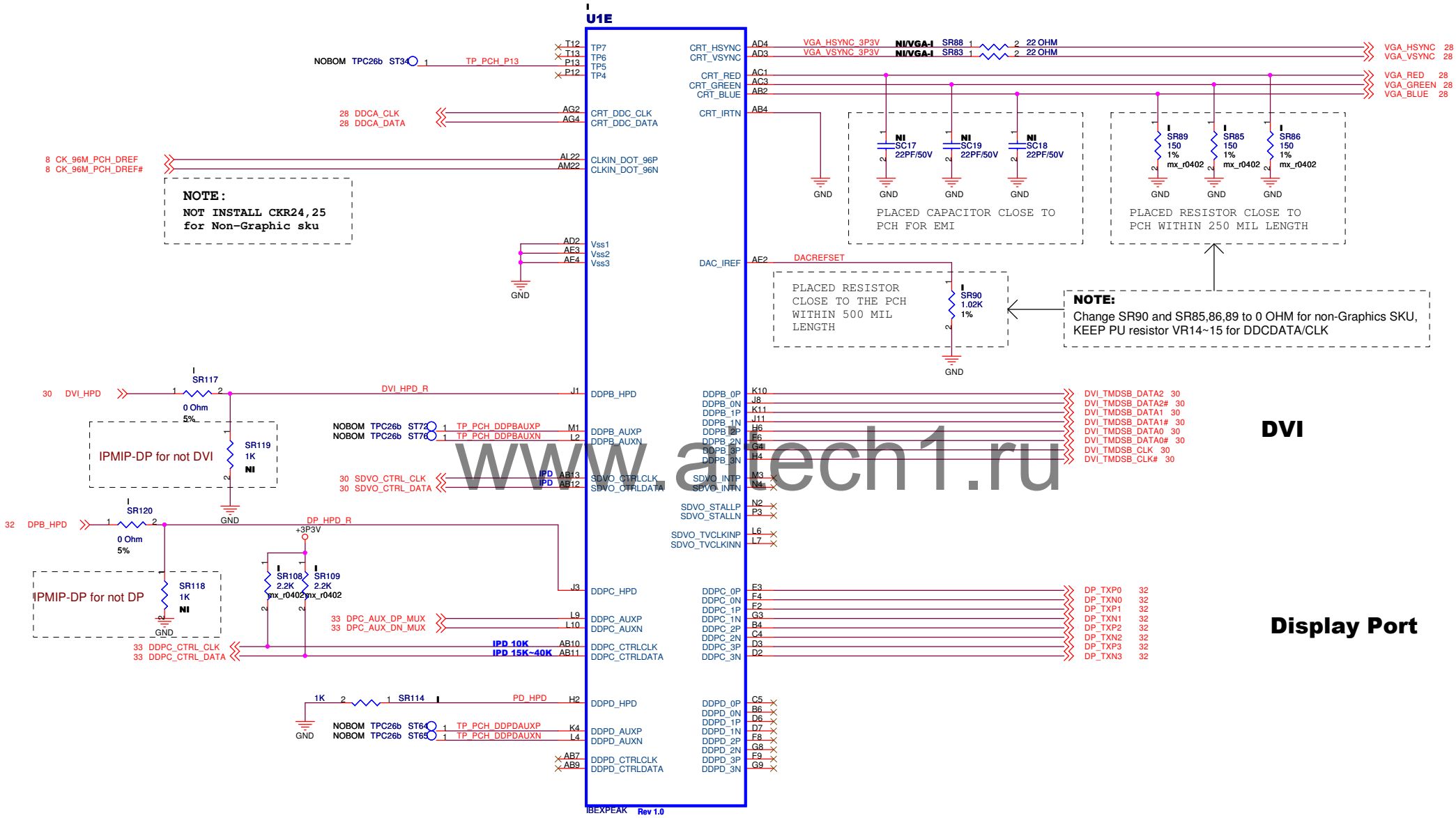
PEGATRON Title : INTEL_PCH - 3

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 21 of 68


NOTE:
Internal Pull-up in PCH
SR87 NI for power sequence t237
GPIO33 | ME update
1-2 | OVERRIDEN
2-3 | DEFAULT
U1D
LPC
AUDIO
IPMIP-GS ADD
IPMIP-GS ADD SC35
JE50:23
MINI_JUMPER
Strap
AZ_SDATA_OUT (IPD)
AZ_SYNC (IPD)
GPIO8 (IPU)
GPIO15 (IPD)
GPIO27 (IPU)
GPIO33
INTVRMEN
SPKR (IPD)
NOTE:
Install for non-Intel LAN support
NOTE:
Just for measure
www.aitech1.ru
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : INTEL_PCH - 4
Pegatron Corp.
Engineer: Vic_Chen
Size A3
Project Name IPMIP-DP
Rev 1.01
Date: Wednesday, April 07, 2010
Sheet 22 of 68



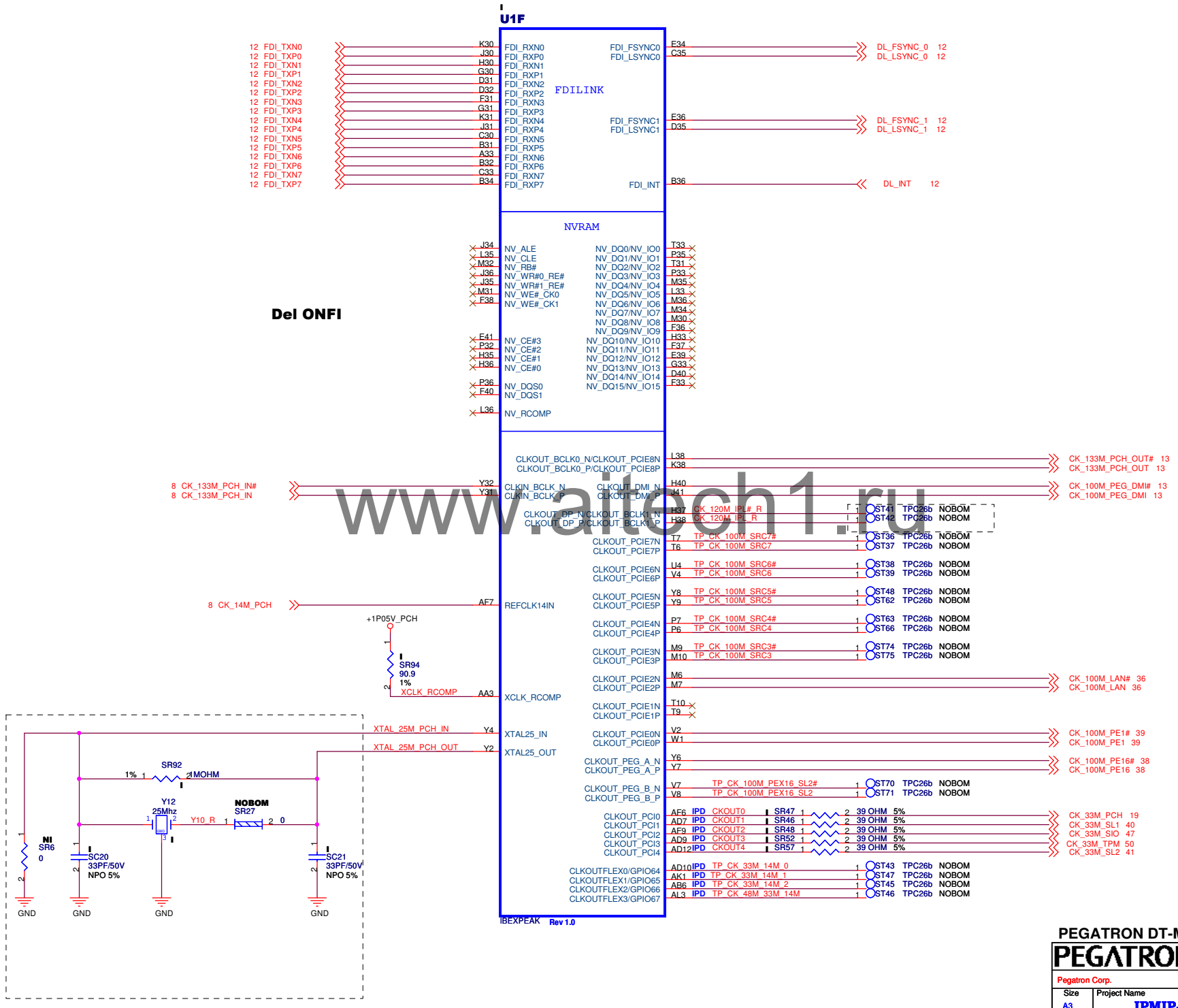
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL_PCH - 5

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 23 of 68



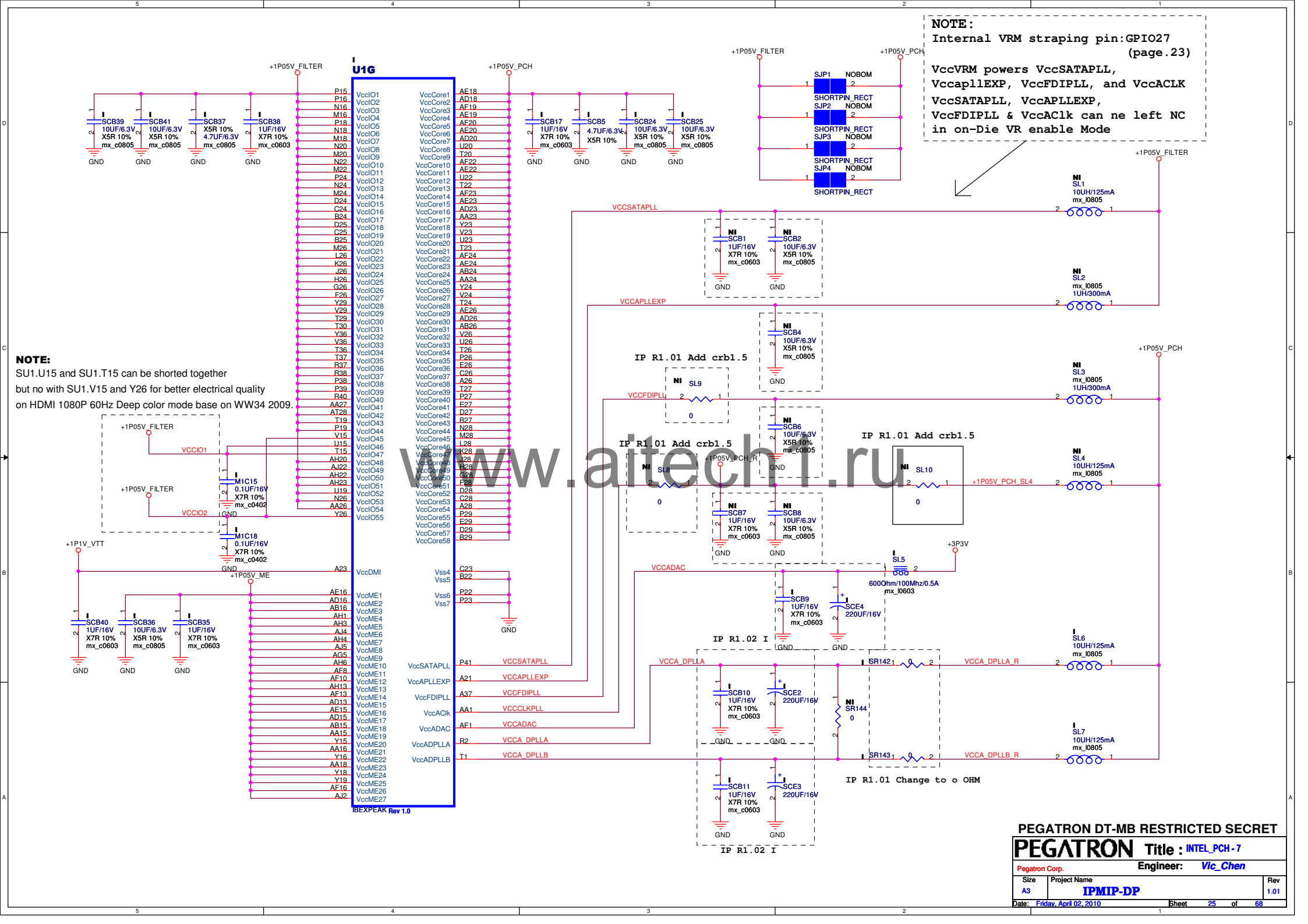
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL_PCH - 6

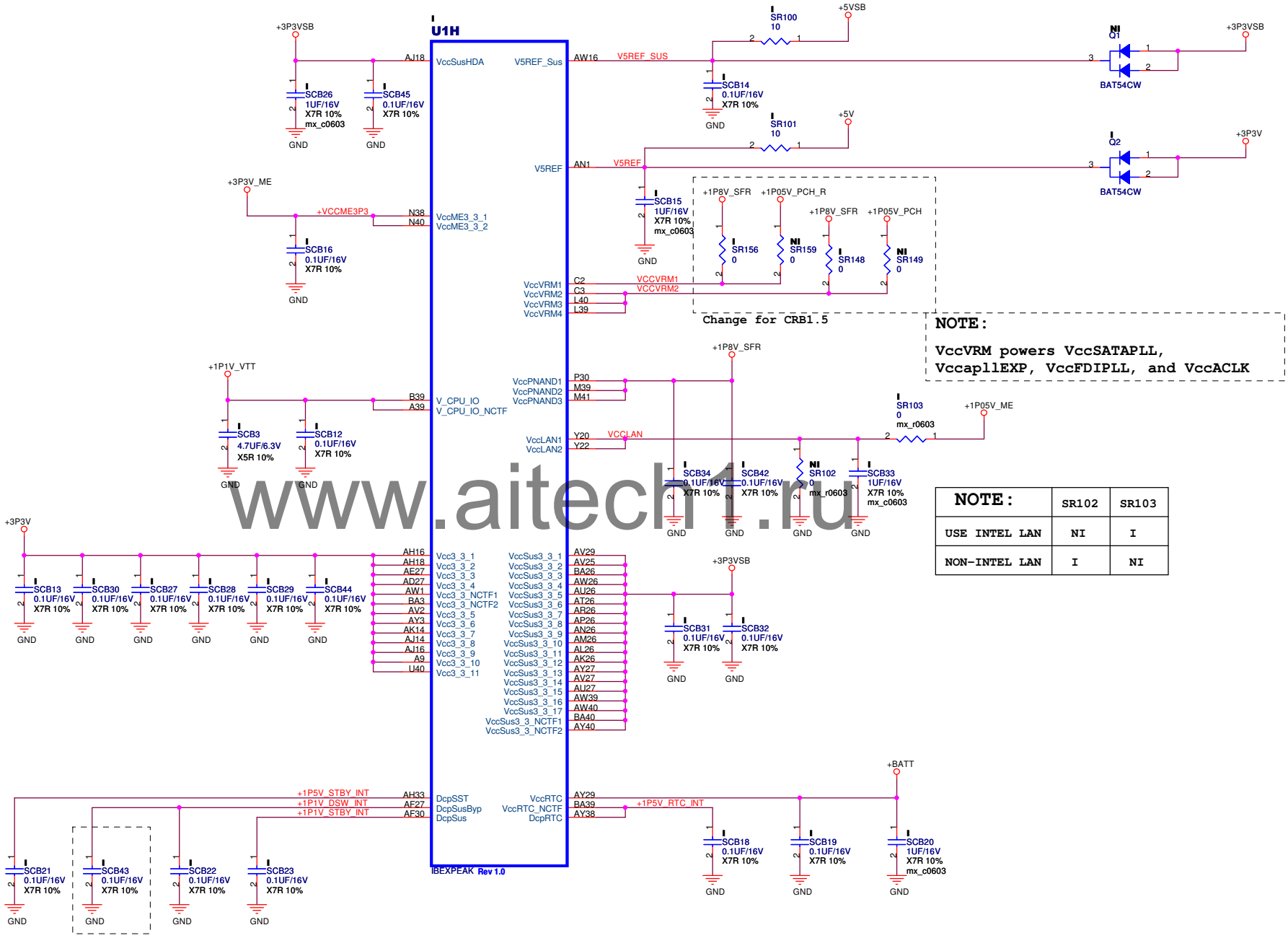
Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 24 of 68


NOTE:
Internal VRM straping pin:GPIO27
(page.23)
VccVRM powers VccSATAPLL,
VccapllEXP, VccFDIPLL, and VccACLK
VccSATAPLL, VccAPLLEXP,
VccFDIPLL & VccAClk can ne left NC
in on-Die VR enable Mode
NOTE:
SU1.U15 and SU1.T15 can be shorted together
but no with SU1.V15 and Y26 for better electrical quality
on HDMI 1080P 60Hz Deep color mode base on WW34 2009.
U1G
IBEXPEAK Rev 1.0
IP R1.01 Add crb1.5
IP R1.01 Add crb1.5
IP R1.01 Add crb1.5
IP R1.02 I
IP R1.02 I
IP R1.01 Change to o OHM
www.aitech1.ru
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : INTEL_PCH - 7
Pegatron Corp. Engineer: Vic_Chen
Size A3 Project Name IPMIP-DP Rev 1.01
Date: Friday, April 02, 2010 Sheet 25 of 68

Note
Place SCB45 close to
SU1.AJ18 for EMI issue



Change for CRB1.5

NOTE:
VccVRM powers VccSATAPLL, VccapllEXP, VccFDIPLL, and VccACLK

NOTE:	SR102	SR103
USE INTEL LAN	NI	I
NON-INTEL LAN	I	NI

NOTE:
MOW WW08 recommand to reserved SCB43.

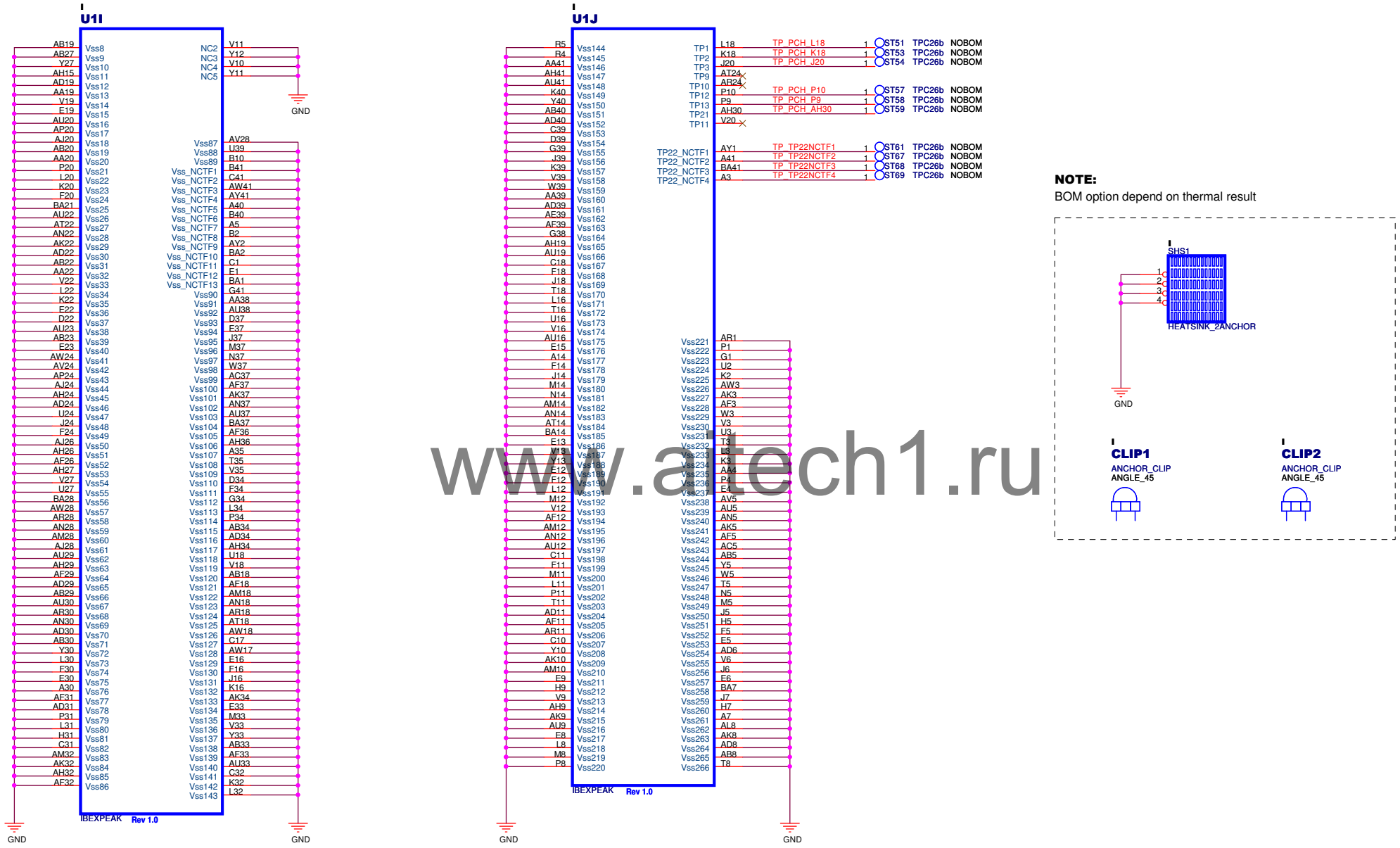
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : INTEL_PCH - 8

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Tuesday, March 23, 2010 Sheet 26 of 68



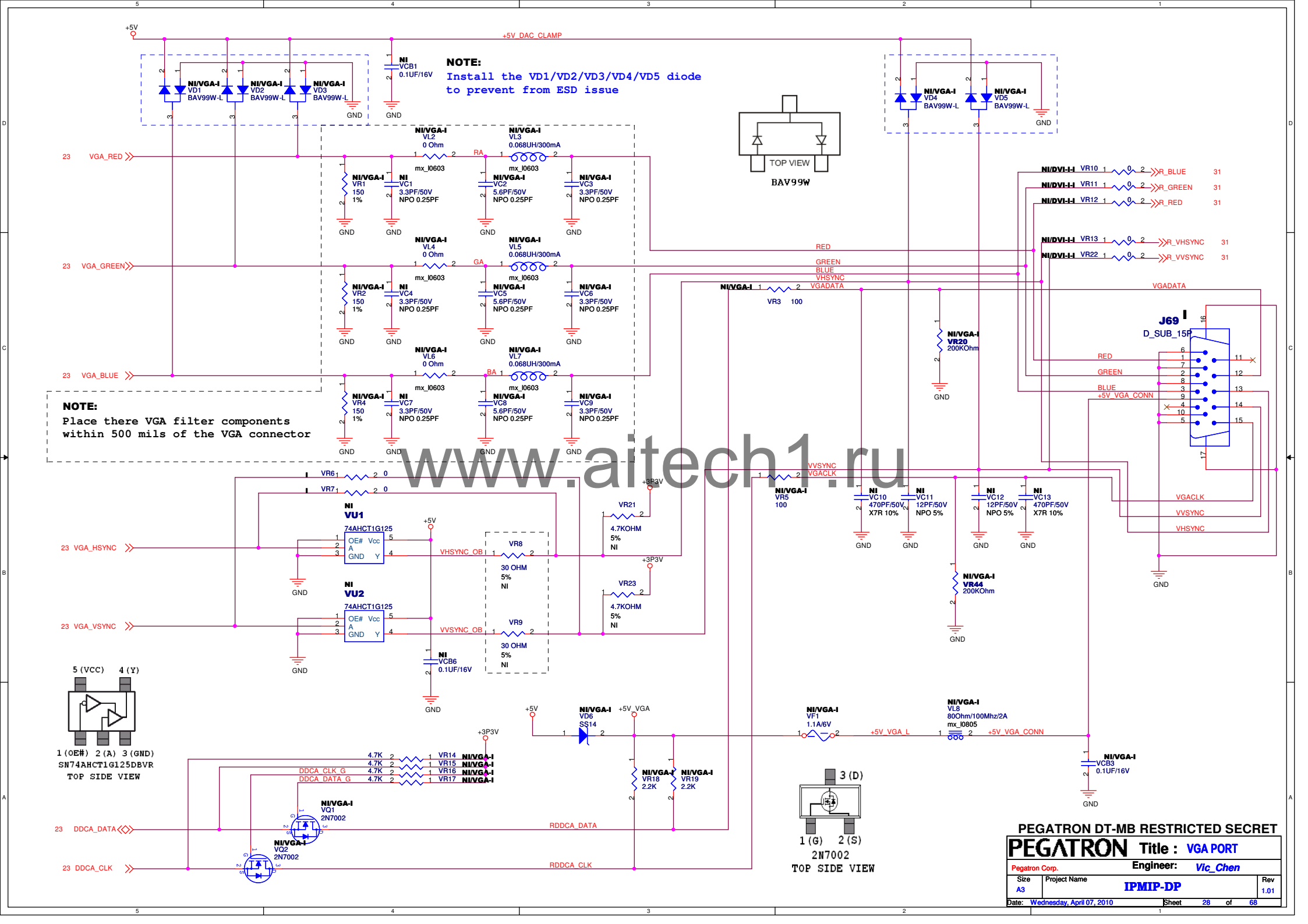
PEGATRON DT-MB RESTRICTED SECRET

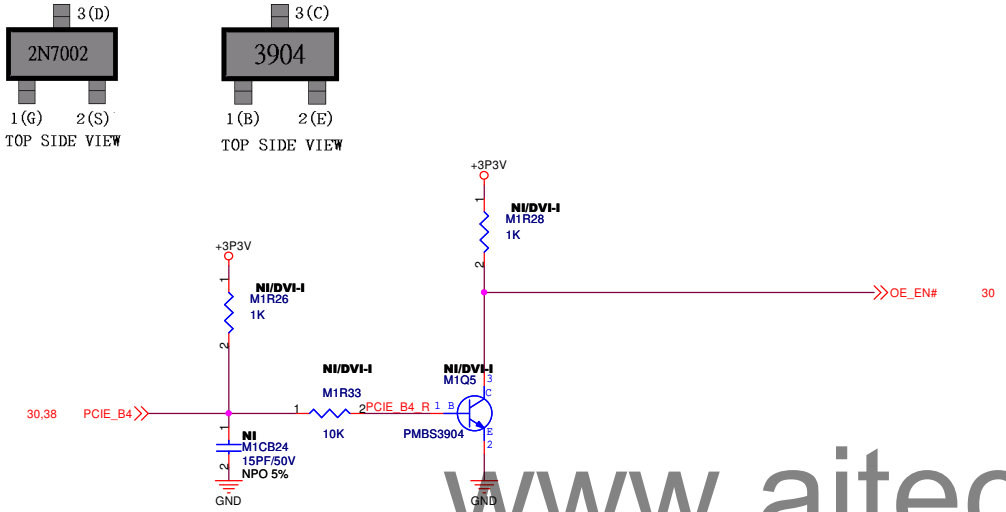
PEGATRON Title : INTEL_PCH - 9

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Tuesday, March 23, 2010 Sheet 27 of 68

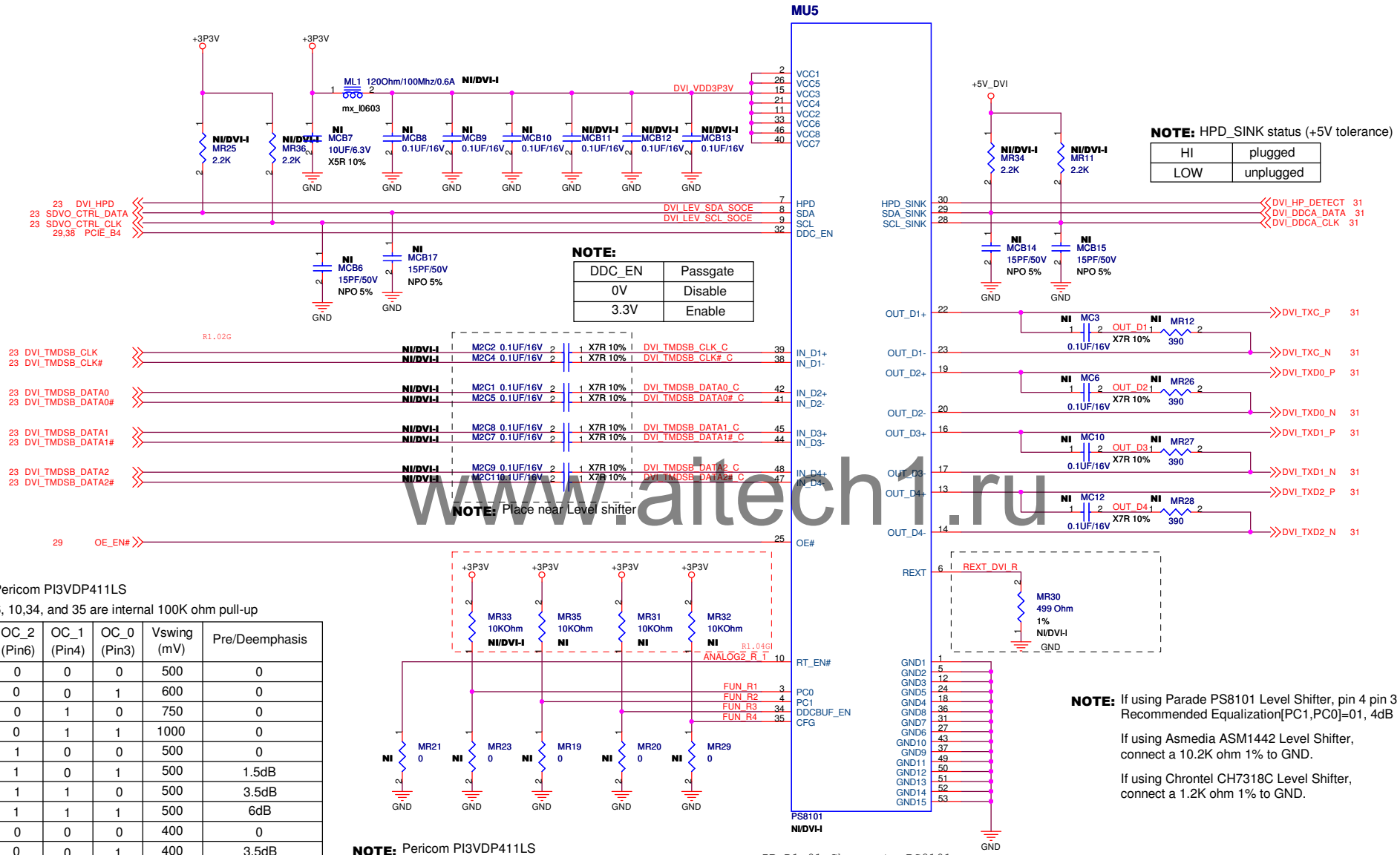

NOTE:
Install the VD1/VD2/VD3/VD4/VD5 diode
to prevent from ESD issue
TOP VIEW
BAV99W
NOTE:
Place there VGA filter components
within 500 mils of the VGA connector
www.aitech1.ru
J69
D_SUB_15P
74AHCT1G125
1(OE#) 2(A) 3(GND)
SN74AHCT1G125DBVR
TOP SIDE VIEW
2N7002
TOP SIDE VIEW
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON
Title : VGA PORT
Pegatron Corp.
Engineer: Vic_Chen
Size A3
Project Name IPMIP-DP
Rev 1.01
Date: Wednesday, April 07, 2010
Sheet 28 of 68



NOTE:

PCIE X16	PCIE_B4	SEL (MUX)	DDC_EN# (Level Shifter)	OE_EN# (Level Shifter)	Function
Plugged	LOW	LOW	LOW	HI	PCIE x16
Unplugged	HI	HI	HI	LOW	DVI , HDMI

CH7318: 02G480001000
ASM1442: 022U-0004000



NOTE: If using Parade PS8101 Level Shifter, pin 4 pin 3 Recommended Equalization[PC1,PC0]=01, 4dB

If using Asmedia ASM1442 Level Shifter, connect a 10.2K ohm 1% to GND.

If using Chrontel CH7318C Level Shifter, connect a 1.2K ohm 1% to GND.

NOTE: Pericom PI3VDP411LS

Pin 3, 4, 6, 10,34, and 35 are internal 100K ohm pull-up

OC_3 (Pin10)	OC_2 (Pin6)	OC_1 (Pin4)	OC_0 (Pin3)	Vswing (mV)	Pre/Deemphasis
0	0	0	0	500	0
0	0	0	1	600	0
0	0	1	0	750	0
0	0	1	1	1000	0
0	1	0	0	500	0
0	1	0	1	500	1.5dB
0	1	1	0	500	3.5dB
0	1	1	1	500	6dB
1	0	0	0	400	0
1	0	0	1	400	3.5dB
1	0	1	0	400	6dB
1	0	1	1	400	9dB
1	1	0	0	1000	0
1	1	0	1	1000	-3.5dB
1	1	1	0	1000	-6dB
1	1	1	1	1000	-9dB

NOTE: Pericom PI3VDP411LS

EQ0 (Pin34)	EQ1 (Pin35)	Equalization (dB)
0	0	3
0	1	7.2
1	0	10
1	1	12

NOTE:

OE*	IN_D Termination	OUT_D Outputs
1	Hi-Z	Hi-Z
0	50ohm	Active

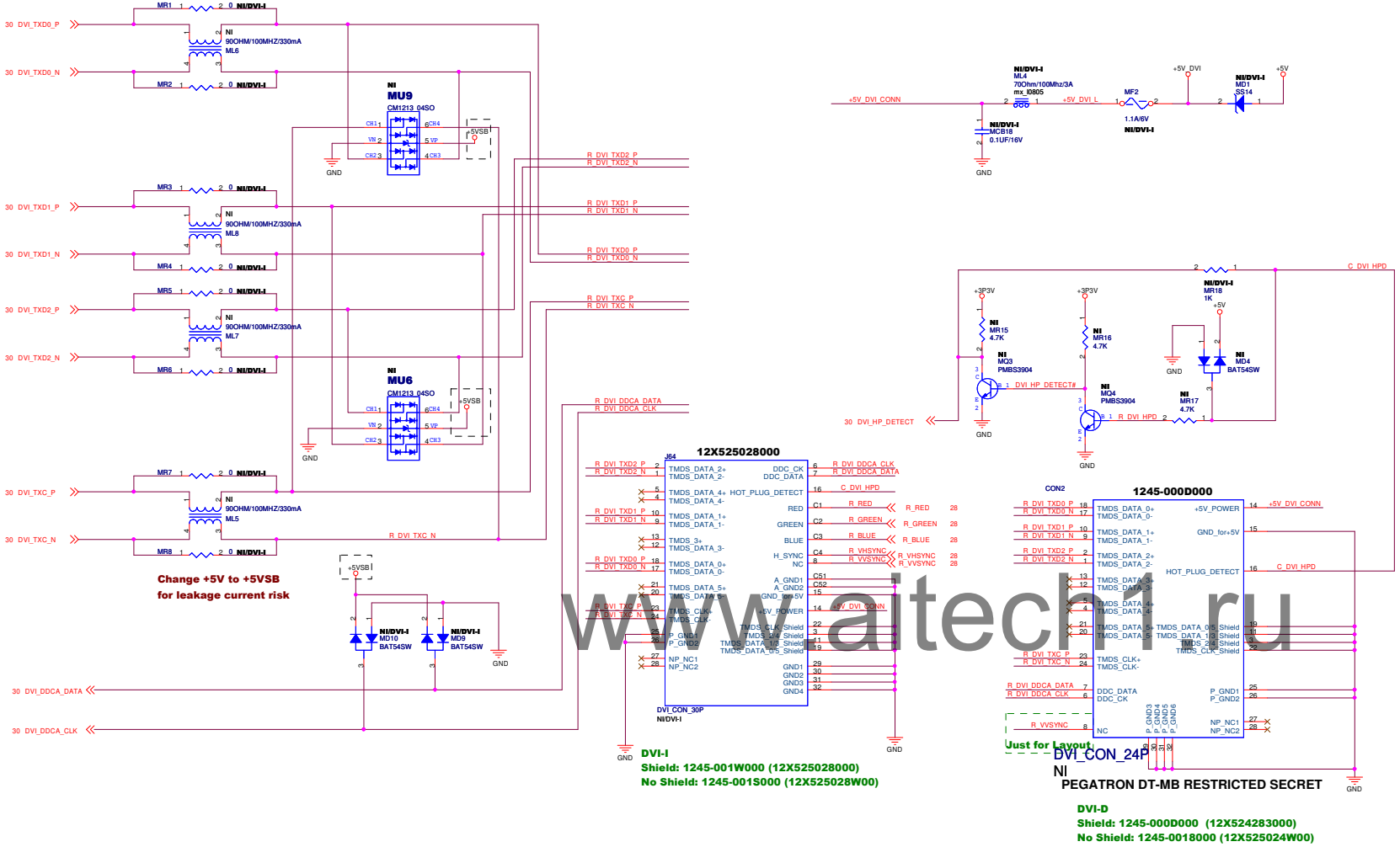
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : DVI Level shifter

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 30 of 68



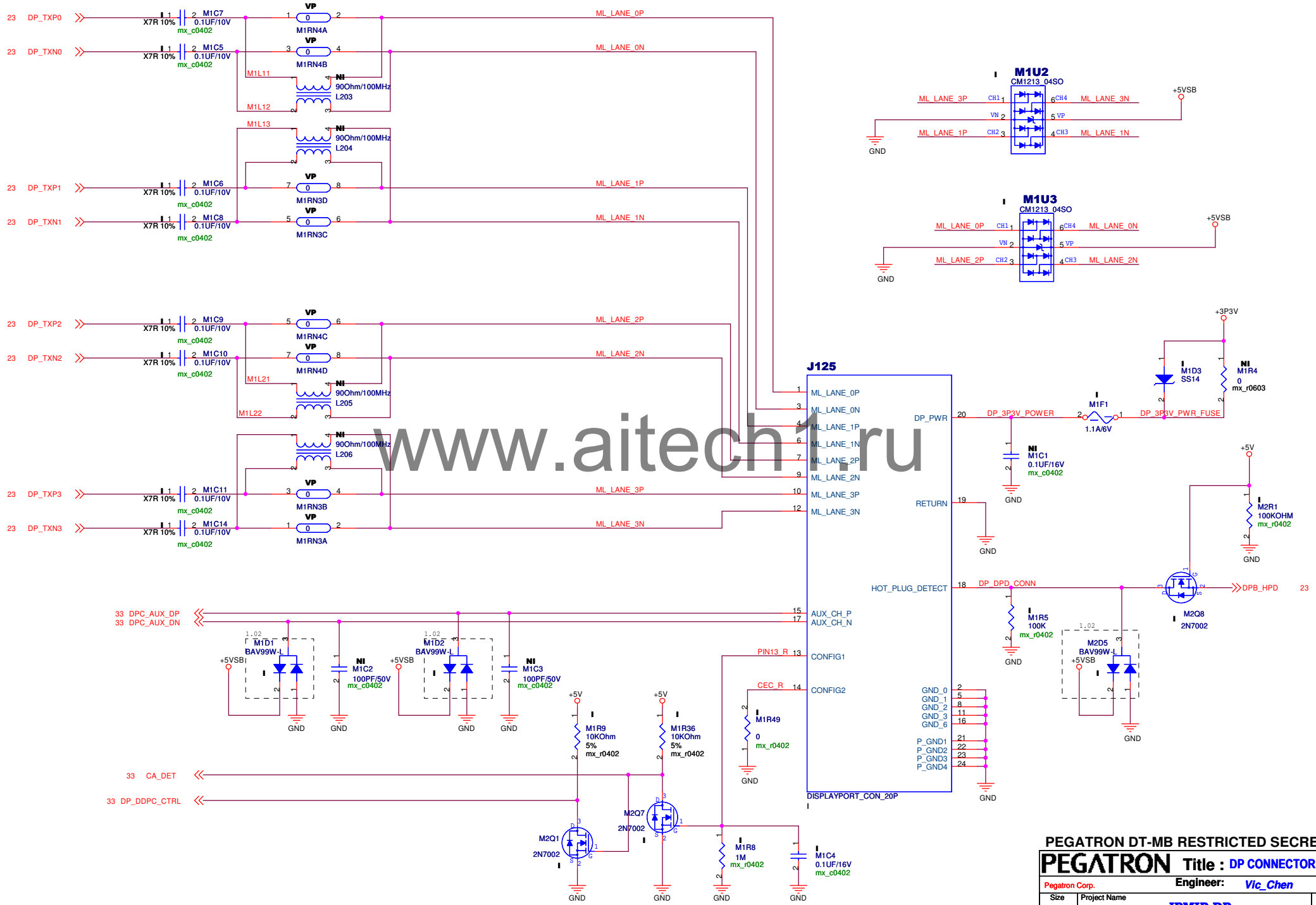
DVI-I
Shield: 1245-001W000 (12X525028000)
No Shield: 1245-001S000 (12X525028W00)

Just for Layout

PEGATRON DT-MB RESTRICTED SECRET

DVI-D
Shield: 1245-000D000 (12X524283000)
No Shield: 1245-0018000 (12X525024W00)

PEGATRON	Title : DVI-I Connector		
Pegatron Corp.	Engineer: Vic_Chen		
Size: A2	Project Name: IPMIP-DP		Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 31 of 68		



PEGATRON DT-MB RESTRICTED SECRET

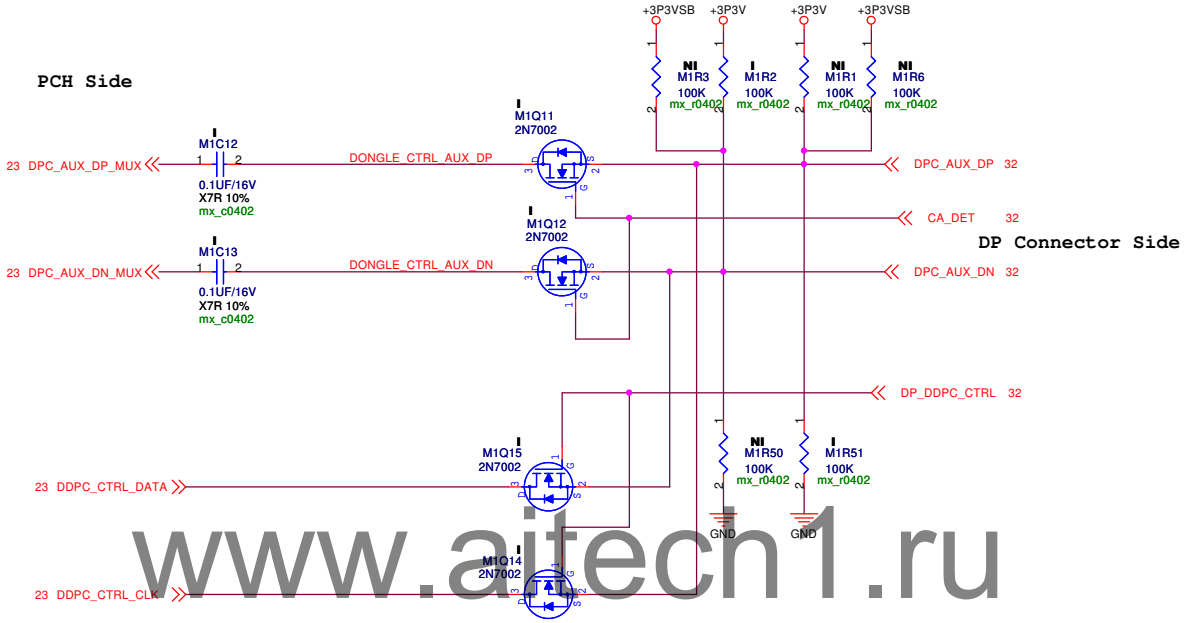
PEGATRON Title : DP CONNECTOR

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

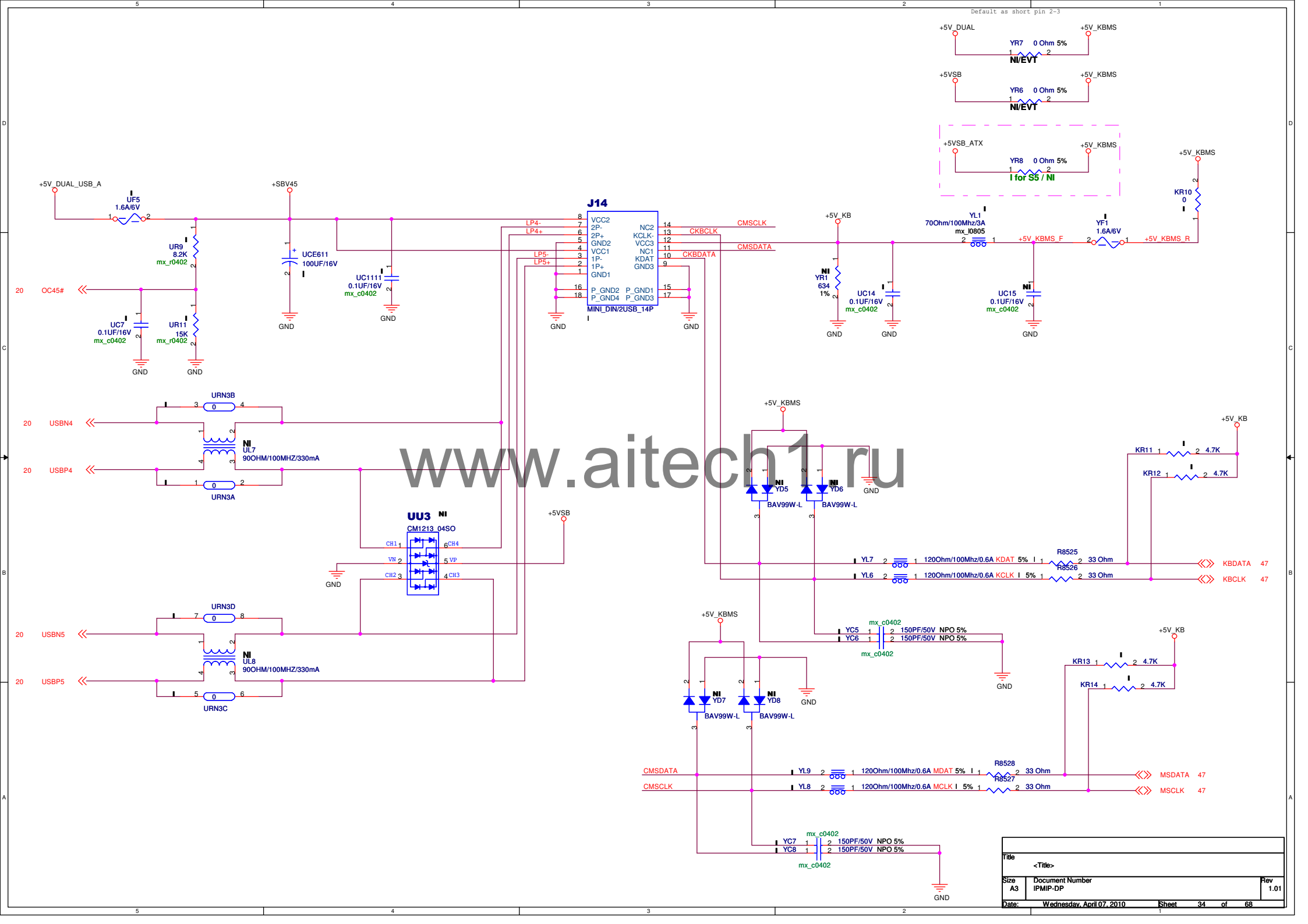
Date: Wednesday, April 07, 2010 Sheet 32 of 68

Display Port to HDMI/DVI Dongle control

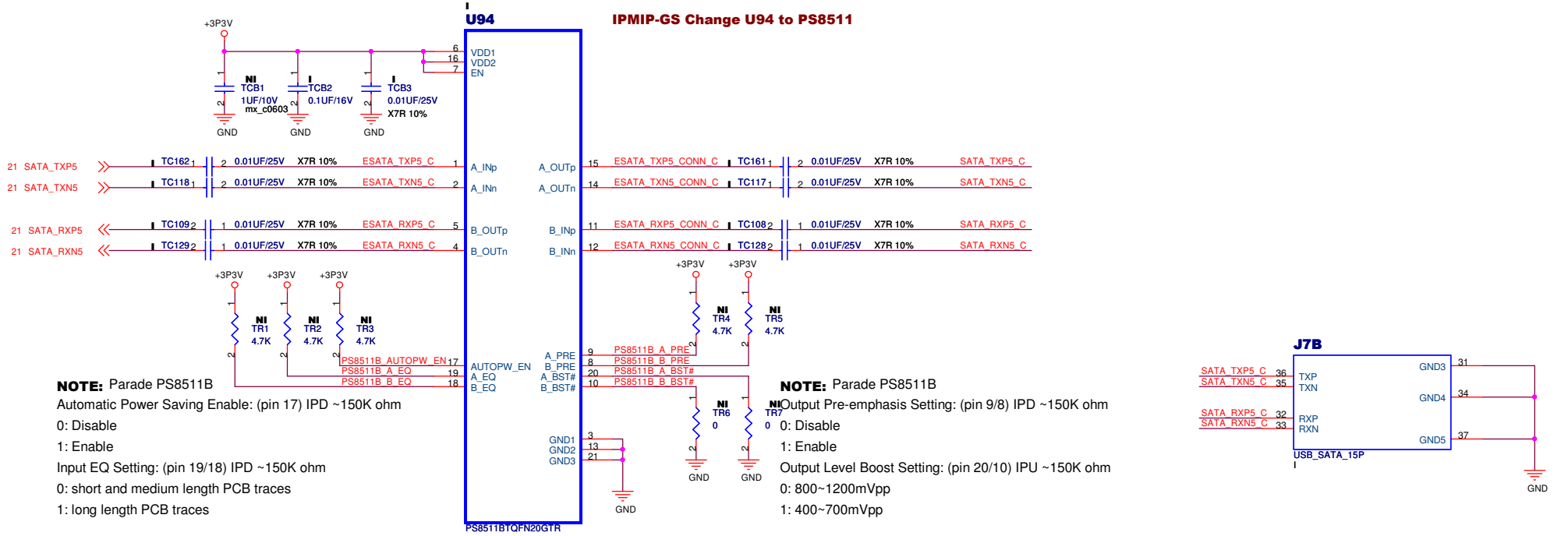


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : DP DONGLE	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 33 of 68	



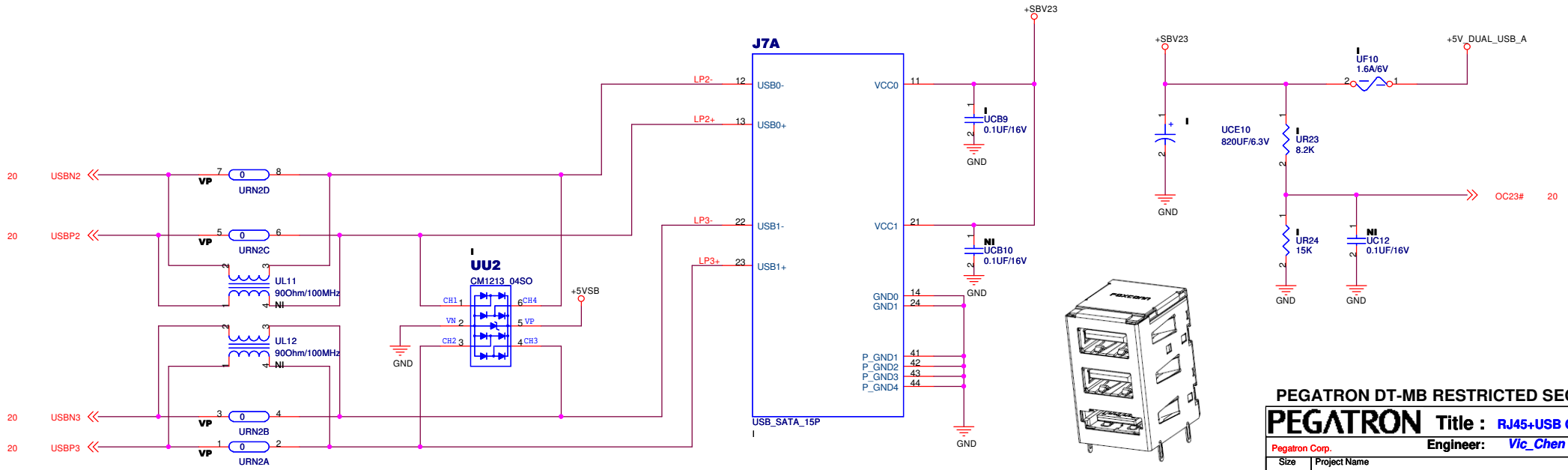
Title	<Title>	
Size A3	Document Number IPMIP-DP	Rev 1.01
Date: Wednesday, April 07, 2010	Sheet 34 of 68	



NOTE: Parade PS8511B
Automatic Power Saving Enable: (pin 17) IPD ~150K ohm
0: Disable
1: Enable
Input EQ Setting: (pin 19/18) IPD ~150K ohm
0: short and medium length PCB traces
1: long length PCB traces

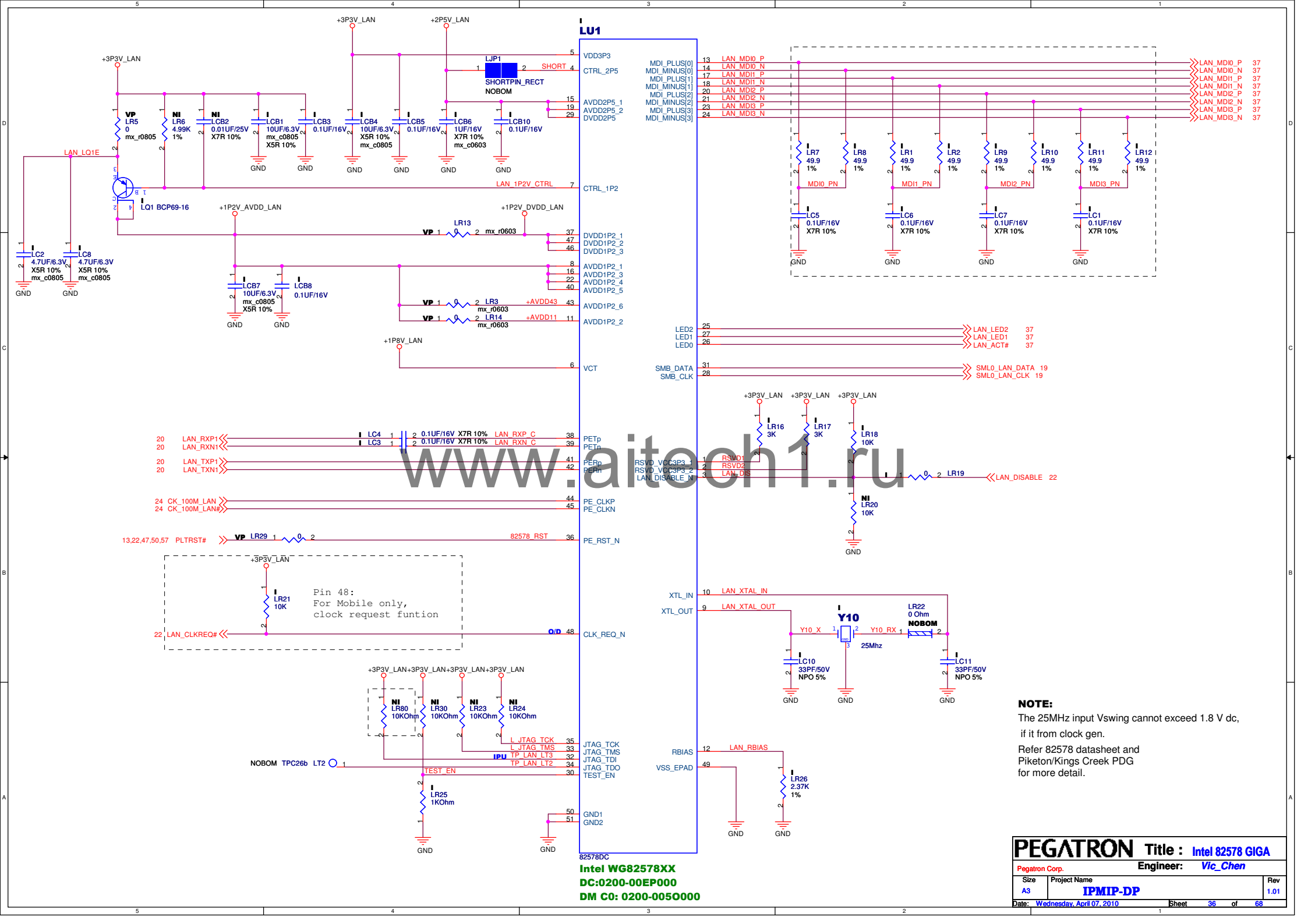
NOTE: Parade PS8511B
Output Pre-emphasis Setting: (pin 9/8) IPD ~150K ohm
0: Disable
1: Enable
Output Level Boost Setting: (pin 20/10) IPU ~150K ohm
0: 800~1200mVpp
1: 400~700mVpp

E-SATA + Dual USB CONNECTOR



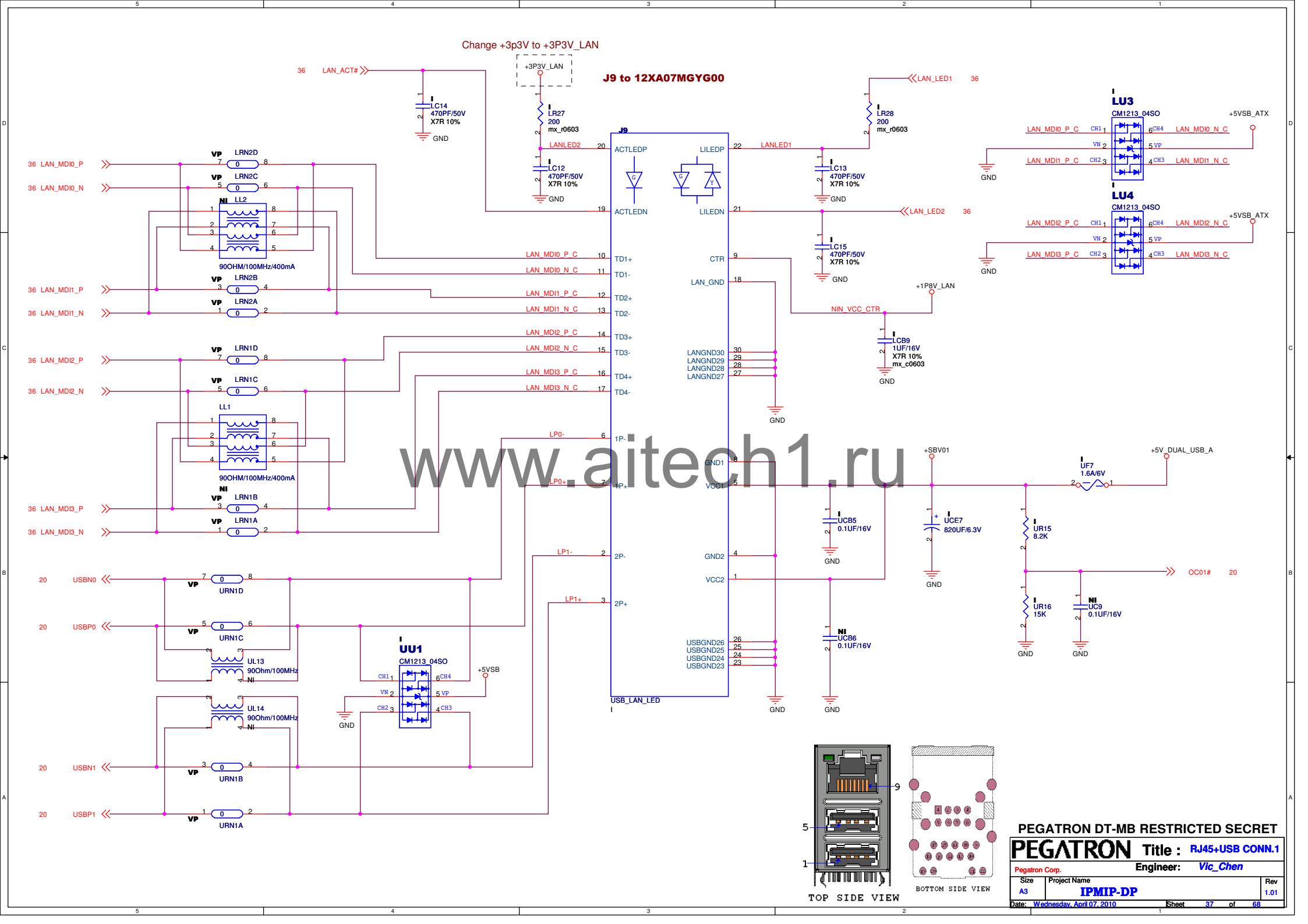
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : RJ45+USB CONN.2	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 35 of 68	



Change +3p3V to +3P3V_LAN

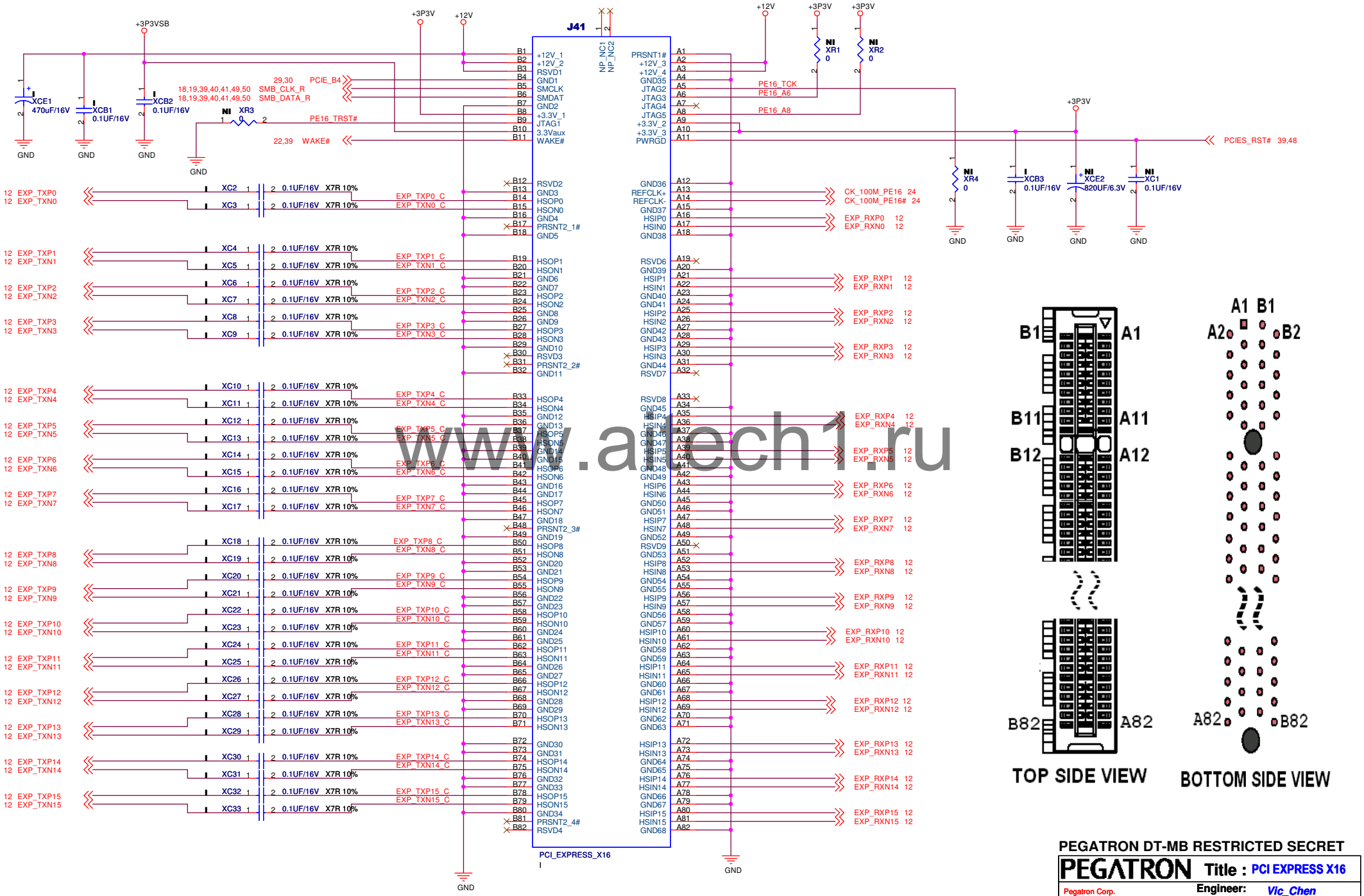
J9 to 12XA07MGYG00



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : RJ45+USB CONN.1	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 37 of 68	

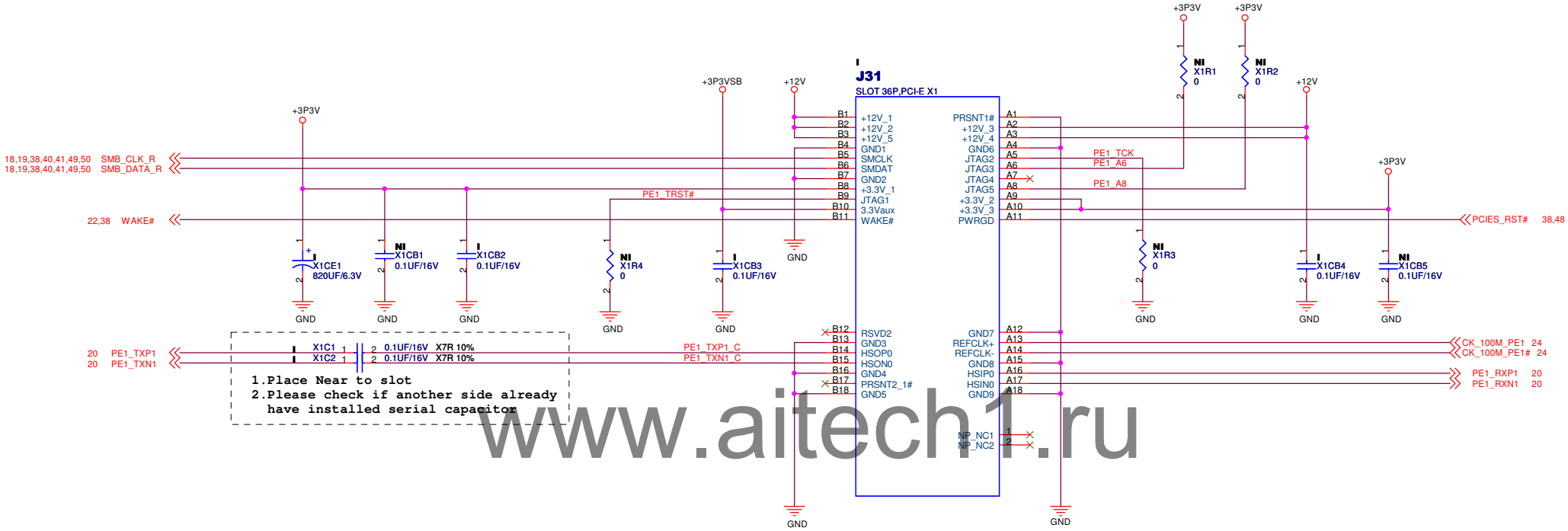
PCI EXPRESS X16 Graphics Card Slot

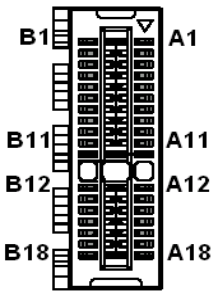


PEGATRON DT-MB RESTRICTED SECRET

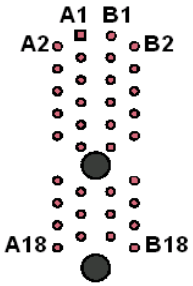
PEGATRON	Title : PCI EXPRESS X16	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 38 of 68	

PCI Express x1 SLOT





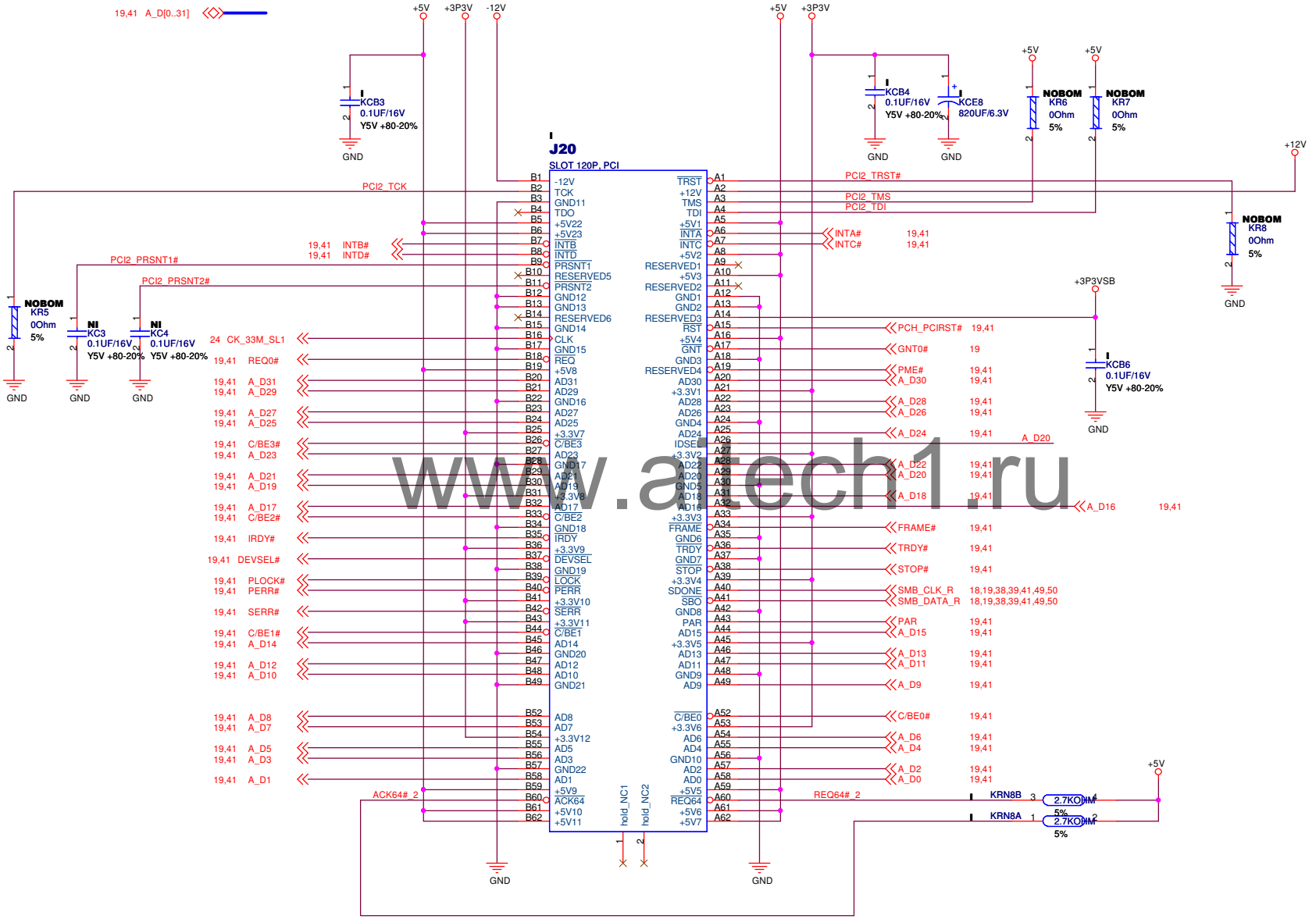
TOP SIDE VIEW



BOTTOM SIDE VIEW

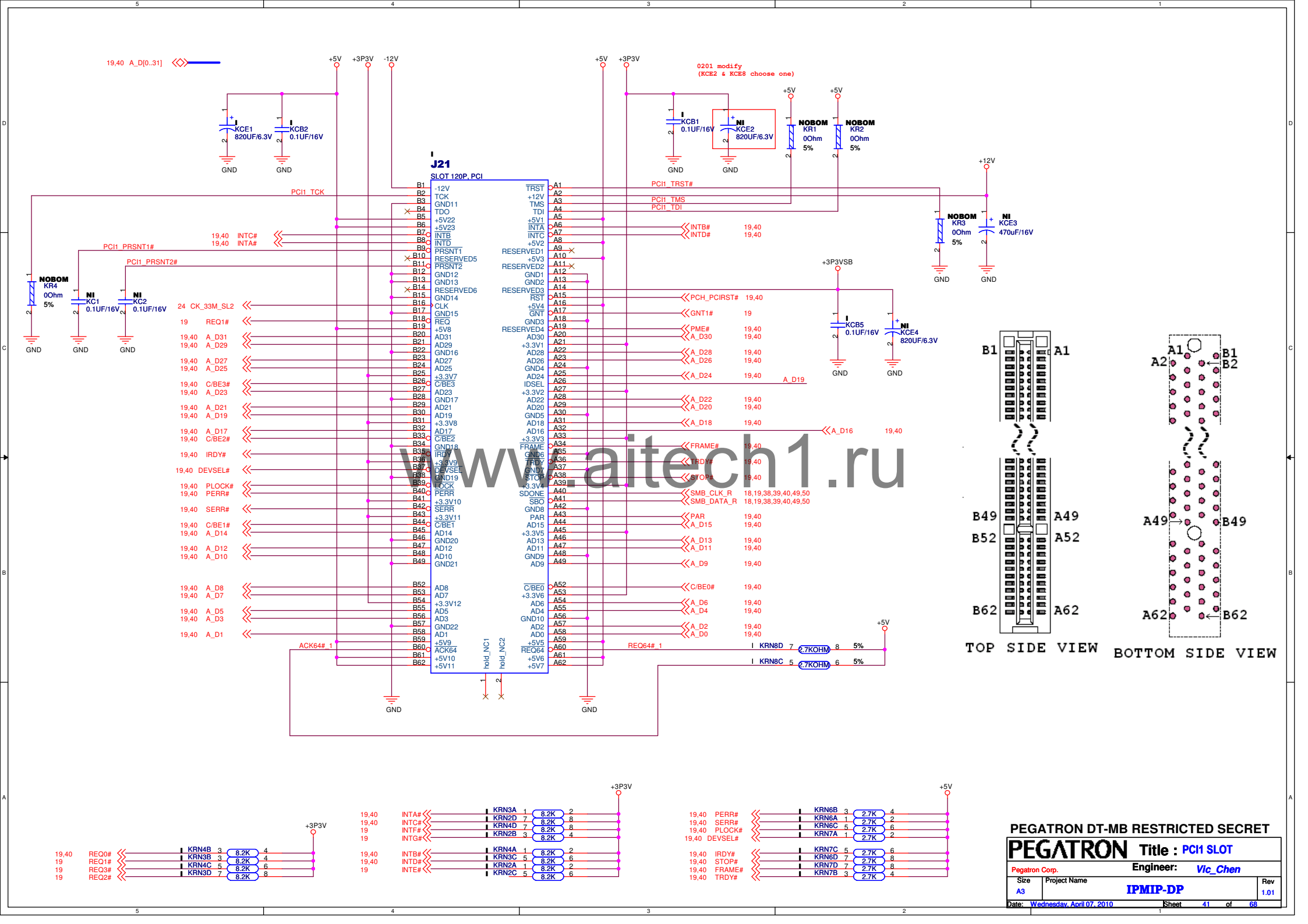
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PCI EXPRESS X1	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 39 of 68	



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : PCI EXPRESS X4	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 40 of 68	



Note : (AD48)

For some power supply , +5VSB drop before +12V when AC power out (S0 --> G3) , +12V will current back to +5VSB If your power supply has this sequence issue , please install AD48 instead of AQ1

Please noite: AZ_BITCLK need add a serial res(22 ohm) near SB side

Digital Region

Provision AR23 for ALC888S-VC codec

PLACE NEAR front audio CODEC FOR EMI

ALC888S_GR

ALC662 02X611003200

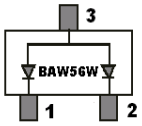
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : AUDIO CODEC

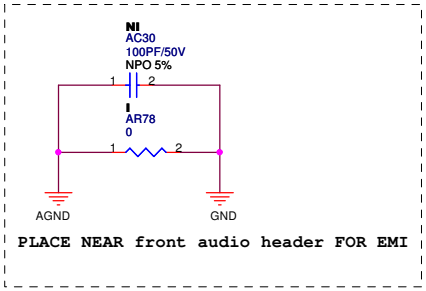
Pegatron Corp. Engineer: Vic_Chen

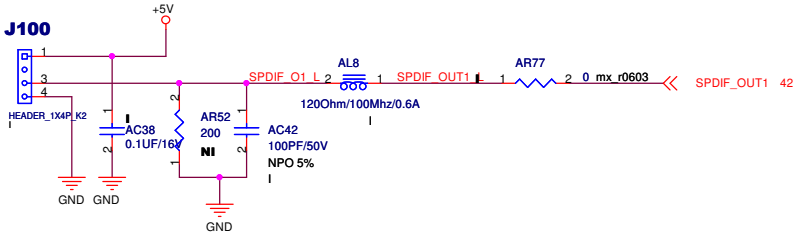
Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 42 of 68



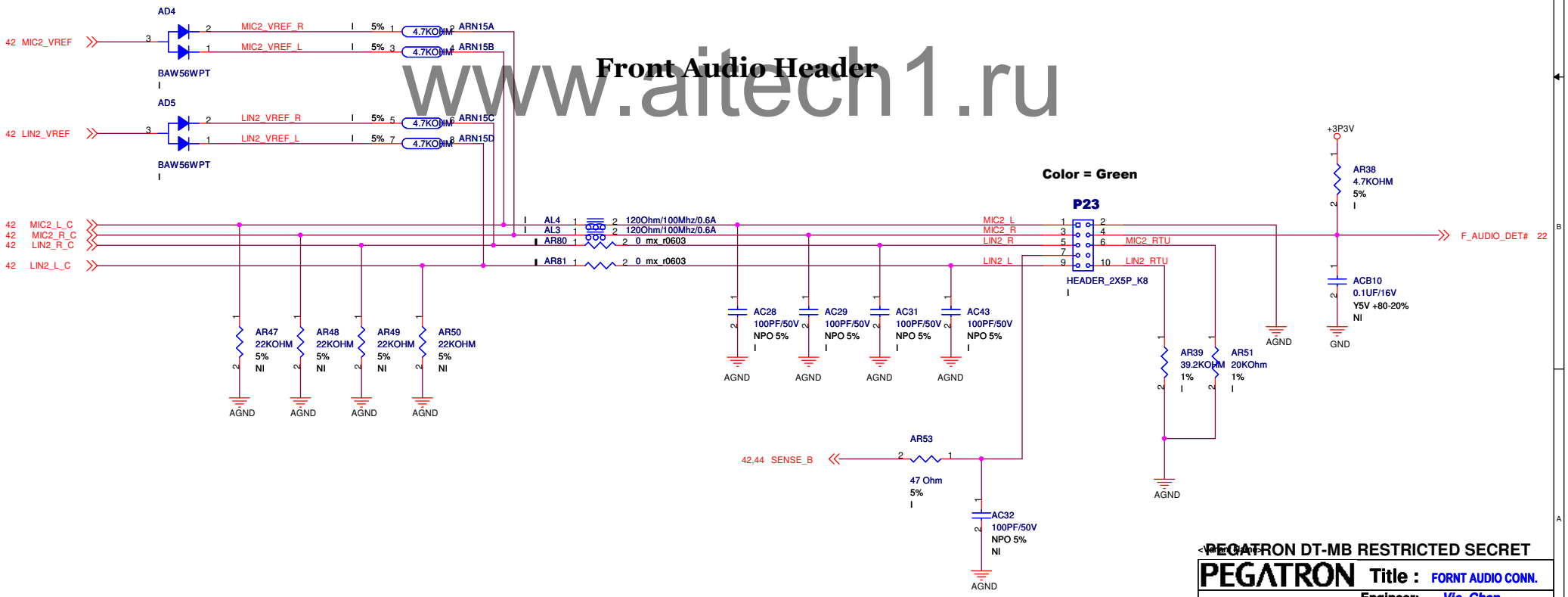
TOP SIDE VIEW





But for other customers (ex, Intel, EPSON, FSC, Dell.....etc), they might don't need 6+3 configuration, just general 6+2 type. If so, please change LINE1 (Pin 23/24) to Rear Line-In port instead of CD-IN, because CD-IN (Pin 18/19/20) port is only dedicated input port and can't retasking

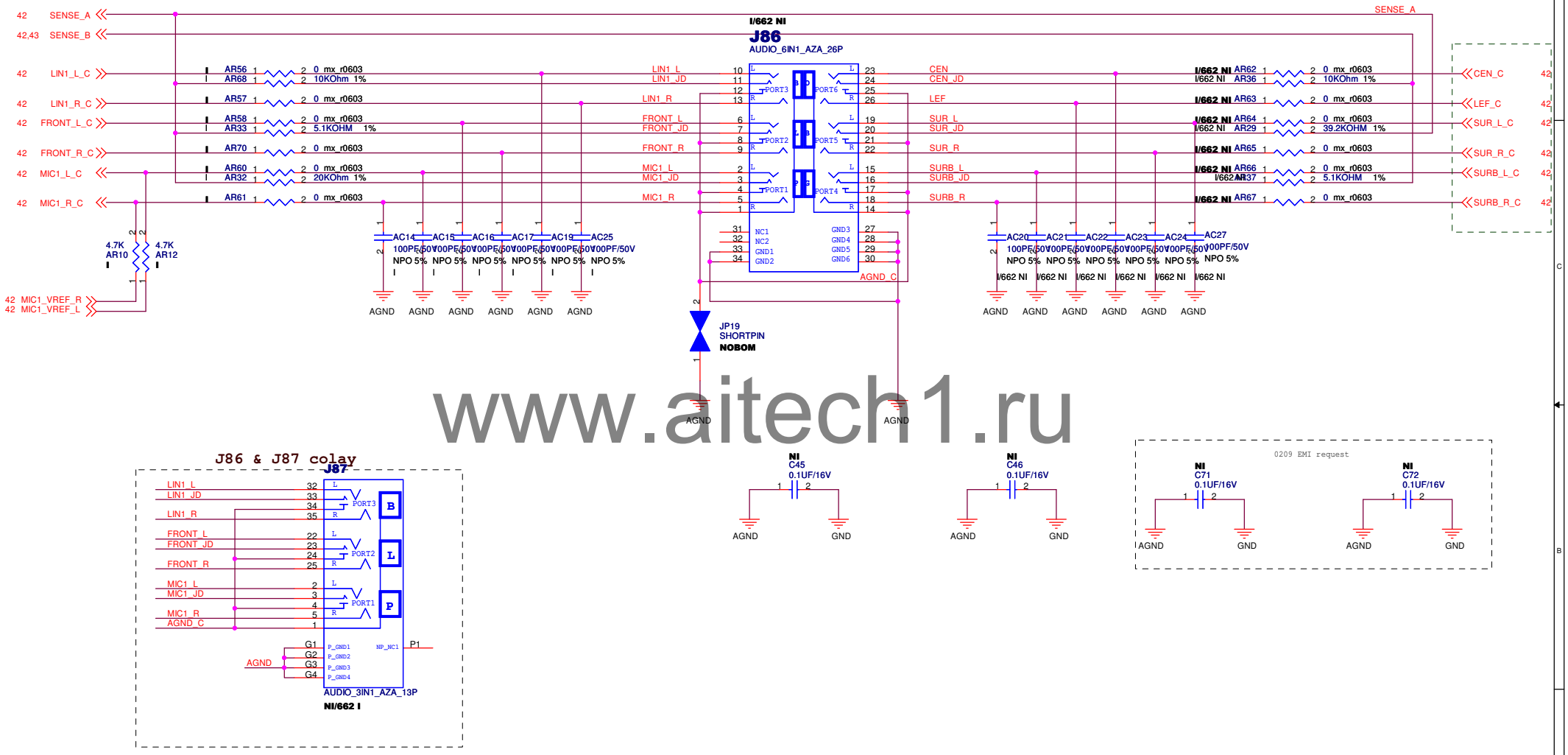
Front Audio Header



PEGATRON	Title : FORNT AUDIO CONN.	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 43 of 68	

Azalia Rear Audio Connector

IPMIP-GS R1.01 Change port



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : REAR AUDIO CONN.	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 44 of 68	

NOTE:
Check USB cable internal whether had capacity
NI:BPC
I: CPC

+SBV89

UCB7 0.1UF/16V

UCE8 470uF/6.3V

UF8 1.6A/6V

+5V_DUAL_USB_B

UR17 8.2K

UR19 15K

NI UC10 0.1UF/16V

OC89# 20

P151 HEADER_2X5P_K9

LP8- LP8 LP9- LP9+

20 USBN8 URN5B

20 USBP8 URN5A

20 USBN9 URN5D

20 USBP9 URN5C

VP

NI 90Ohm/100MHz UL3

NI 90Ohm/100MHz UL4

UU5 CM1213_04SO

CH1 VN CH2 CH4 VP CH3

+5VSB

GND

SRV05 4
TOP SIDE VIEW

NOTE:
Check USB cable internal whether had capacity
NI: BPC
I: CPC

+SBV1011

UCB8 0.1UF/16V

UCE9 470uF/6.3V

UF9 1.6A/6V

+5V_DUAL_USB_B

UR20 8.2K

UR22 15K

NI UC11 0.1UF/16V

OC1011# 20

P152 HEADER_2X5P_K9

LP10- LP10+ LP11- LP11+

20 USBN10 URN6B

20 USBP10 URN6A

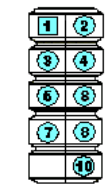
20 USBN11 URN6D

20 USBP11 URN6C

NI 90Ohm/100MHz UL5

NI 90Ohm/100MHz UL6

UU6 CM1213_04SO



TOP SIDE VIEW

BOTTOM SIDE VIEW

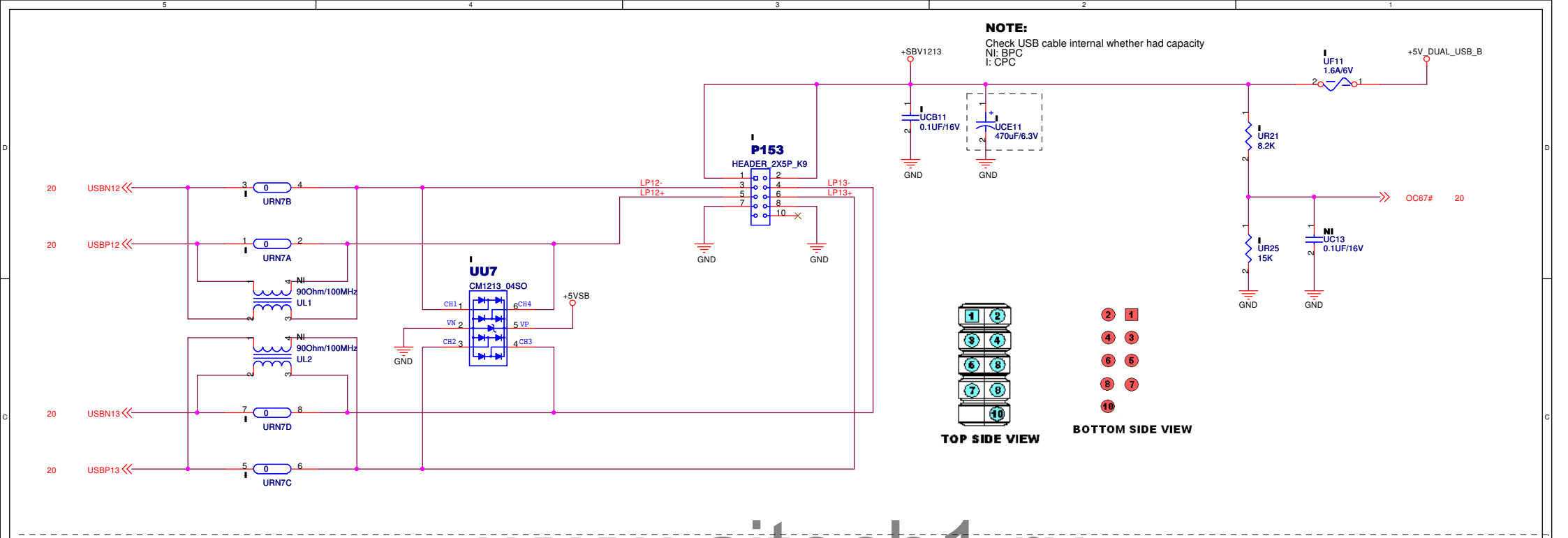
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : USB HEADER CON.

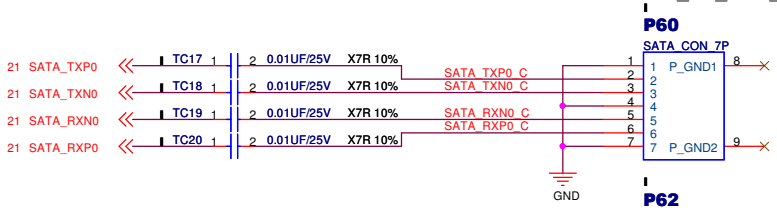
Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

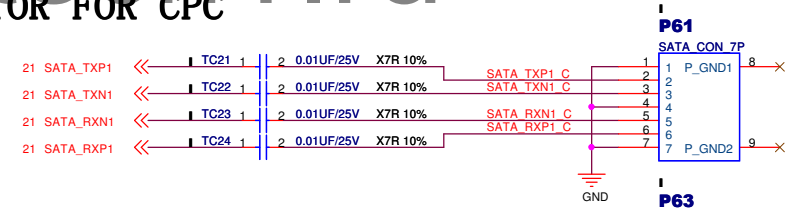
Date: Wednesday, April 07, 2010 Sheet 45 of 68



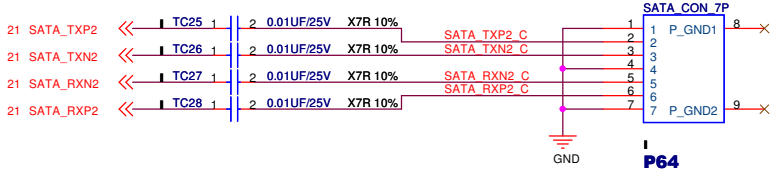
SATA CONNECTOR FOR CPC



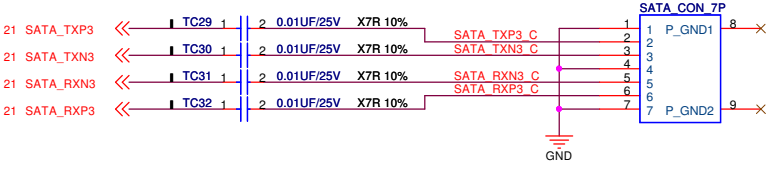
SATA CONTROLLER #1
(PRIMARY MASTER)
COLOR = RED



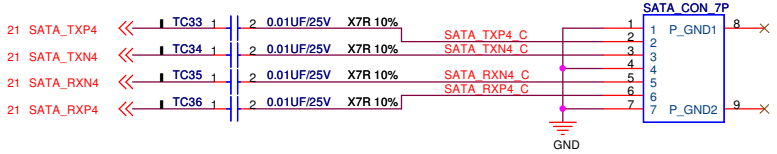
SATA CONTROLLER #1
(SECONDARY MASTER)
COLOR = RED



SATA CONTROLLER #1
(PRIMARY MASTER)
COLOR = RED



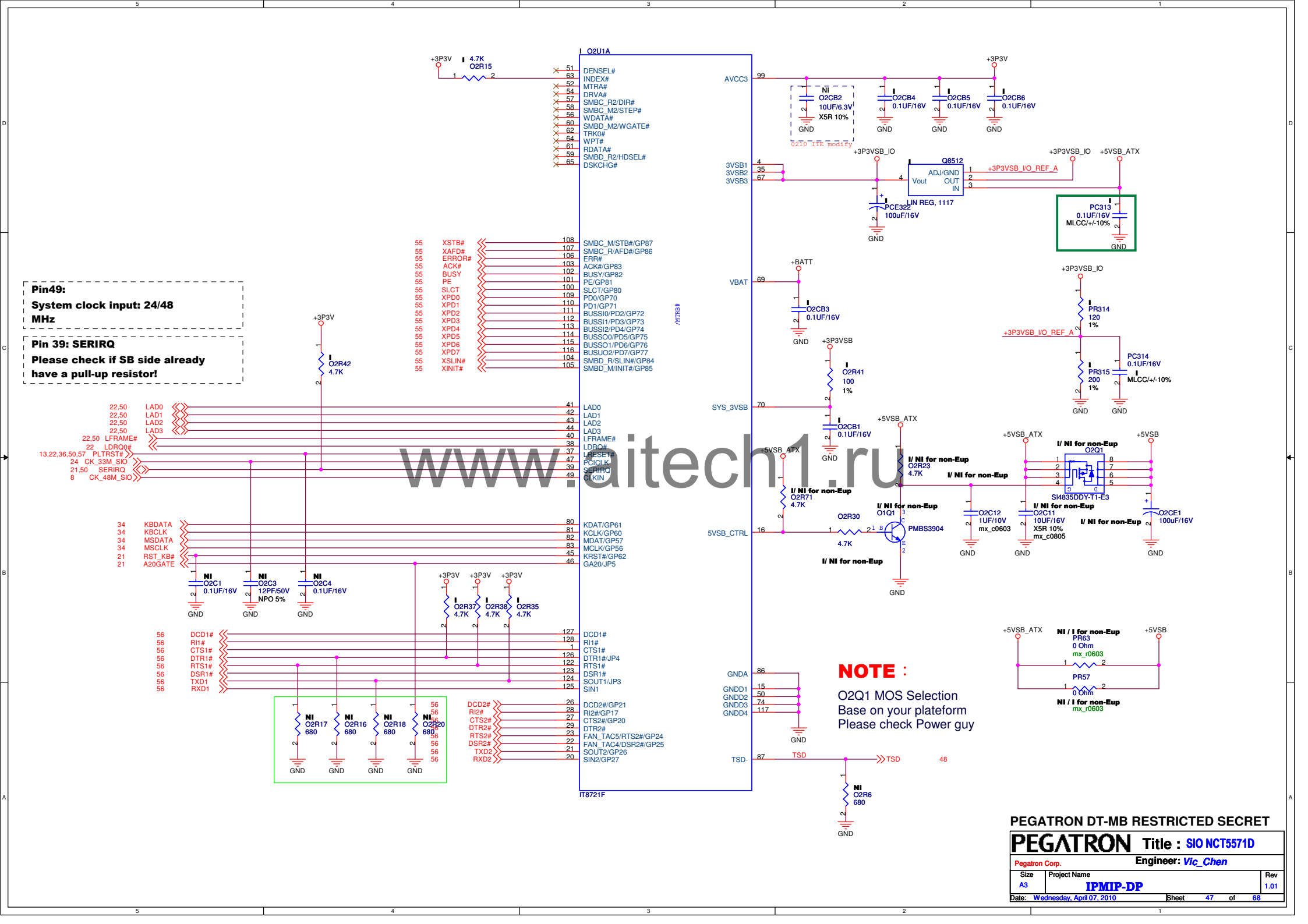
SATA CONTROLLER #1
(SECONDARY MASTER)
COLOR = RED

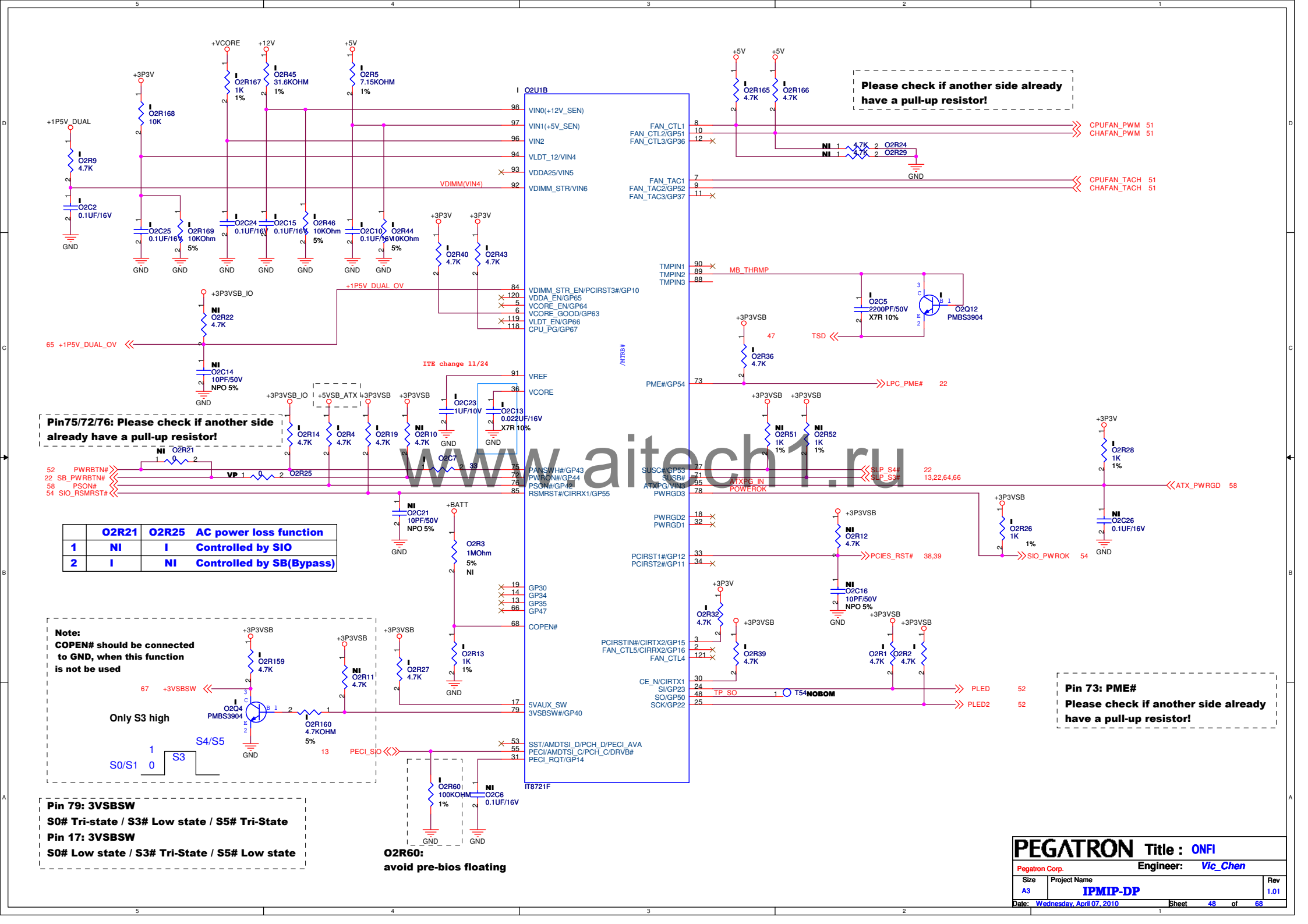


SATA CONTROLLER #2
(PRIMARY MASTER)
COLOR = RED

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : USB HEADER CON.	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 46 of 68	


Pin49:
System clock input: 24/48 MHz
Pin 39: SERIRQ
Please check if SB side already have a pull-up resistor!
O2U1A
IT8721F
NOTE :
O2Q1 MOS Selection
Base on your plateform
Please check Power guy
www.aitech1.ru
PEGATRON DT-MB RESTRICTED SECRET
PEGATRON Title : SIO NCT5571D
Pegatron Corp.
Engineer: Vic_Chen
Size A3
Project Name IPMIP-DP
Rev 1.01
Date: Wednesday, April 07, 2010
Sheet 47 of 68



	O2R21	O2R25	AC power loss function
1	NI	I	Controlled by SIO
2	I	NI	Controlled by SB(Bypass)

PEGATRON	Title : ONFI		
Pegatron Corp.	Engineer: Vic_Chen		
Size: A3	Project Name: IPMIP-DP		Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 48 of 68		

SM BUS Control

To PCH, PCI, and PCIE Slot

18,19,38,39,40,41,50 SMB_DATA_R

18,19,38,39,40,41,50 SMB_CLK_R

To Clock Gen, DIMMs, and ITP Debug Port

SMB_DATA_M 8,16,17,57

SMB_CLK_M 8,16,17,57

+3P3V

VP R14 0

NI R18 2.7K

NI R19 2.7K

NI Q7 2N7002

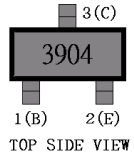
VP R39 0

NI Q14 2N7002

+12V

NI R15 8.2K

PWROK_R_Q



TOP SIDE VIEW

SPI BIOS ROM - 64Mbit

19 SPI_CS#

19 SPI_MISO

19 SPI_MOSI

19 SPI_CLK

E16 HEADER_2X4P_K4

+3P3V_ME

F3R5 8.2K

NI F3R1 0

GND

U14 SOCKET_8P NI

SPI_CS# E16

SPI_MISO

FWH_WP#

SPI_HOLD#

F3R6 8.2K

F3CB1 0.1UF/16V

JE16:12

MINI_JUMPER

IPMIP-GS Change SPI to 64Mb

64Mb: 05X00Z2GE330

32Mb:05X00Z2FC330

16Mb 05X00Z2EA330

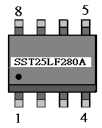
U96 W25Q64BVSSIG

SPI_CLK

SPI_MOSI

BOTTOM SIDE VIEW

TOP SIDE VIEW



TOP SIDE VIEW

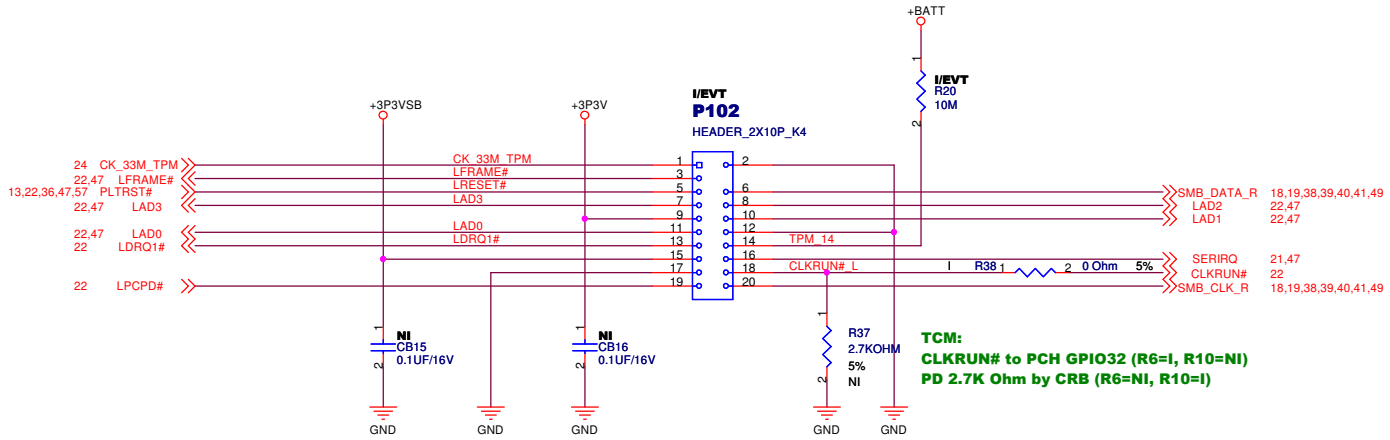
PEGATRON DT-MB RESTRICTED SECRET

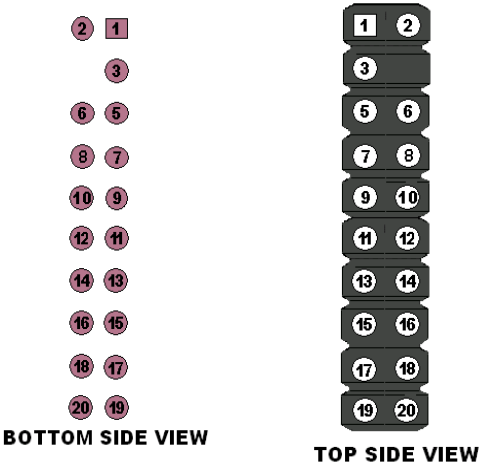
PEGATRON Title : SPI FLASH - 8M

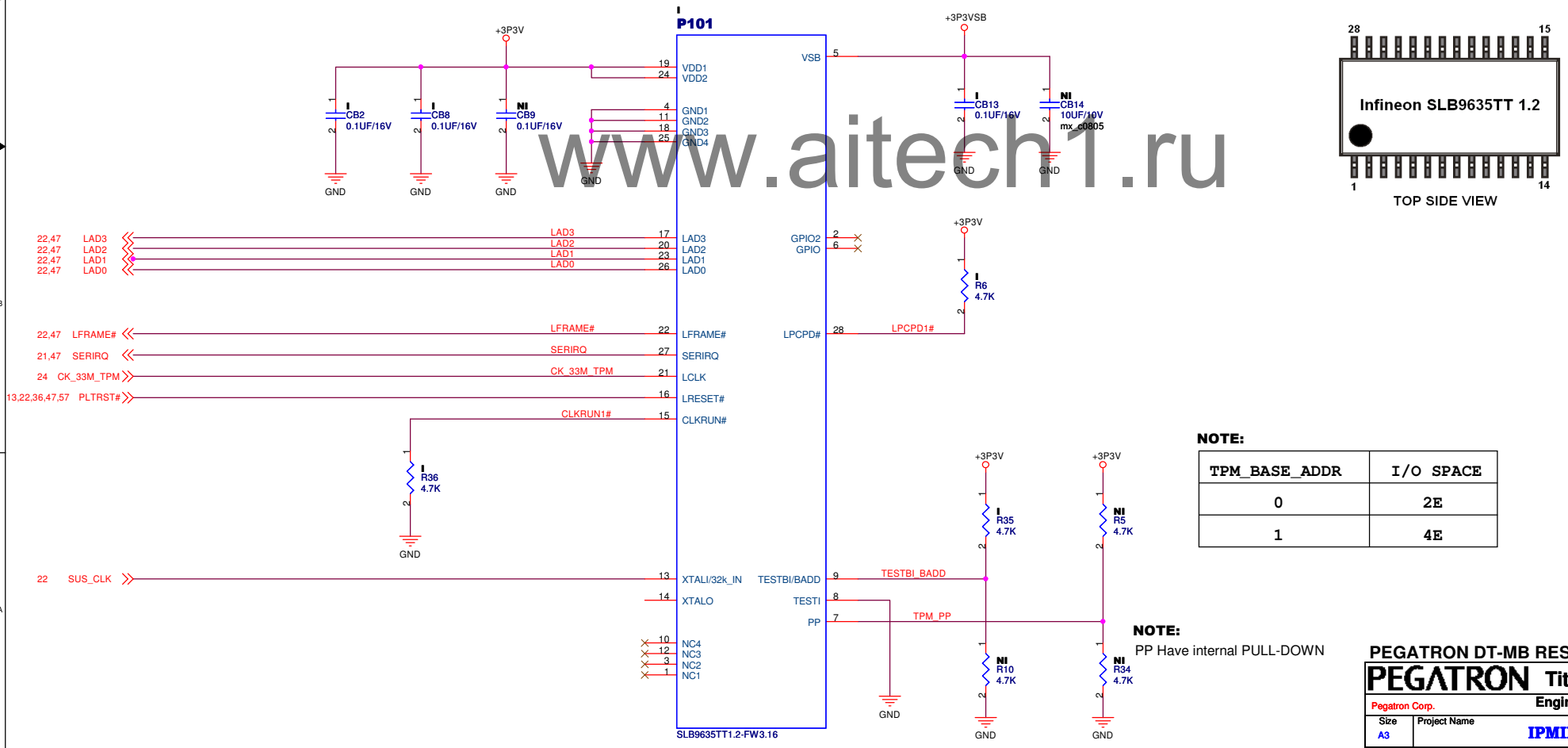
Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 49 of 68







NOTE:

TPM_BASE_ADDR	I/O SPACE
0	2E
1	4E

NOTE:
PP Have internal PULL-DOWN

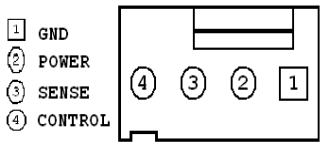
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : SATA2 & TPM/TCM

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 50 of 68

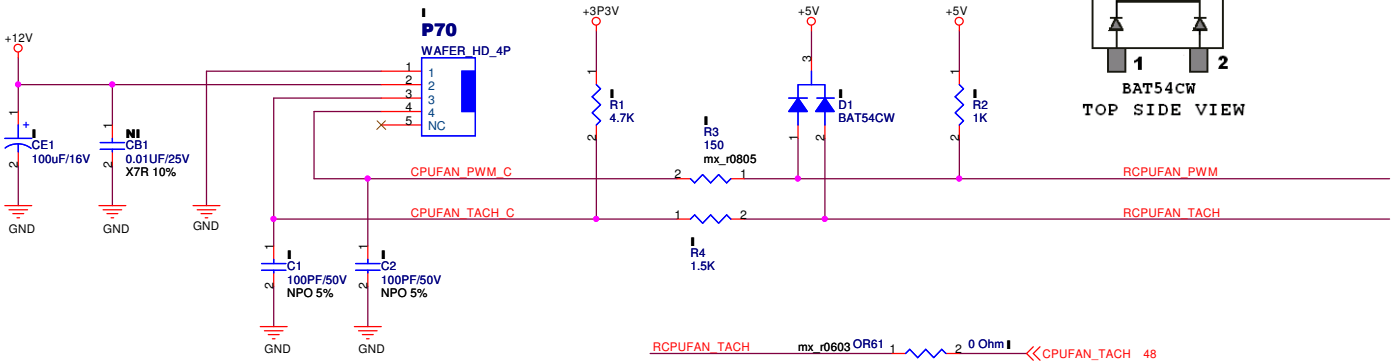


TOP SIDE VIEW

BOTTOM SIDE VIEW

CPU FAN
COLOR: WHITE
W/POST

P70
WAFER_HD_4P

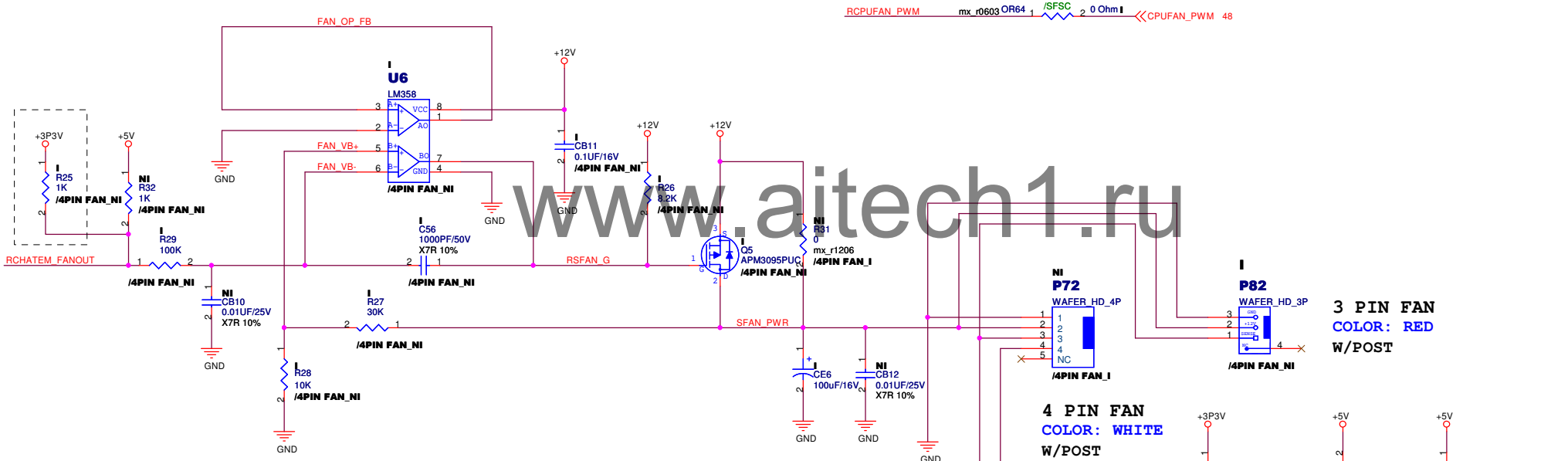


BAT54CW
TOP SIDE VIEW

RCPUFAN_TACH mx_r0603 OR61 0 Ohm CPUFAN_TACH 48

RCPUFAN_PWM mx_r0603 OR64 /SFSC 0 Ohm CPUFAN_PWM 48

3 & 4 PIN CO-LAYOUT Circuit (Default 3 pin fan)

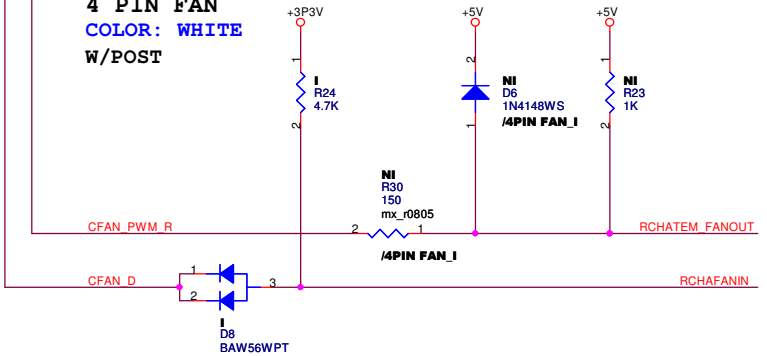


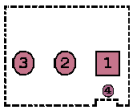
NI P72
WAFER_HD_4P
/4PIN FAN_I

P82
WAFER_HD_3P
/4PIN FAN_NI

3 PIN FAN
COLOR: RED
W/POST

4 PIN FAN
COLOR: WHITE
W/POST

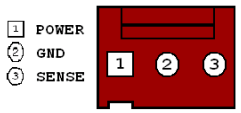




BOTTOM SIDE VIEW

RCHAFANIN OR52 0 Ohm mx_r0603 /NB_FAN/AFSC CHAFAN_TACH 48

RCHATEM_FANOUT OR56 0 Ohm mx_r0603 /NB_FAN/AFSC CHAFAN_PWM 48



TOP SIDE VIEW

3 PIN FAN
COLOR: RED
W/POST

R1.03G

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : 4-PIN FAN CONN

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Thursday, April 08, 2010 Sheet 51 of 68

+5VSB : GREEN

+5VSB
I/EVT
R21
300
mx_r0603
CR1_R
I/EVT
CR1
GREEN
SMD
GND

BUZZER

I=5/(220+40)=19.2mA
P=I*I*R=19.2*19.2*220
=0.0811W=1/12.33 W

+5V
R12
220 Ohm
5%
I/EVT
BUZZ1_R
SPKO
P7
AC_1205G
I/EVT
40Ohm
Max 40mA
P13
HEADER_1X4P_K2
NI
GND
R13
33 Ohm
5%
I
Q88_R56
Q18
PMBS3904
I
R11
4.7KOHM
5%
I
22
SPKR
CB346
0.1UF/16V
Y5V +80-20%
NI
GND
GND

INTRUDER

+BATT
+5VSB
P305
HEADER_1X4P_K2
I/EVT/chas_intru
R_INTRUDER#
R17
10MOhm
5%
I/EVT/chas_intru
R22
10MOhm
5%
NI
INTRUDER#
22
Q56
2N7002
I/EVT/chas_intru
GND
GND

JP305:34
MINI_JUMPER
I/EVT

HPD CONTROL PANEL / LED CIRCUITRY

+5V_DUAL
I
O3R1
220
mx_r0805
NI/Dual I
O3Q1
PMBS3904
NI/Dual I
O3R2
1K
SIO_LED1_G
+3P3VSB
NI
O3R13
1K
NI
O3C5
0.1UF/16V
PLED2
48
GND
GND

+3P3V
+3P3VSB
I
O3R4
8.2K
NI
O3R12
4.7K
21
HD_LED#
8,13,22,57
SYS_RESET#
FP_SYS_RST#
I
O3R9
33
I
O3C1
0.1UF/16V
GND

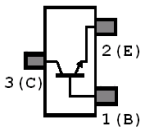
+5V
I
O3R3
220
mx_r0805
I
P5
HEADER_2X5P_K10
HDLED+
FP_LED+
FP_LED-
FP_PWRBTN#
GND
GND

+3P3VSB
I
O3R5
4.7K
I
O3R8
33
I
O3C2
1000PF/50V
X7R 10%
NI
O3C3
0.1UF/16V
NI
O3C4
0.1UF/16V
GND
GND
GND

PWRBTN#
48

+5V_DUAL
I
O3R6
220
mx_r0805
I
O3Q2
PMBS3904
I
O3R11
1K
SIO_LED2_G
+3P3VSB
NI
O3R7
1K
PLED
48
NI
O3R10
0
mx_r0805
GND
GND
GND

FRONT POWER LED COLOR SUPPORT	O3Q1	O3R2			
SINGLE COLOR	NI	NI			
DUAL COLOR	I	I			



PMBS3904
TOP SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

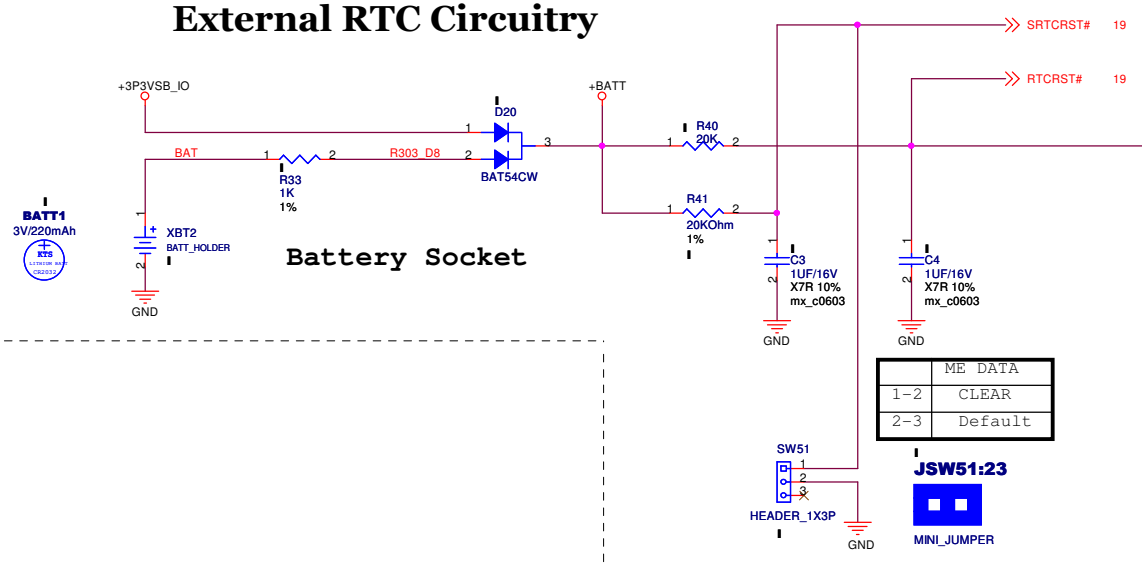
PEGATRON Title : FRONT PANEL

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 52 of 68

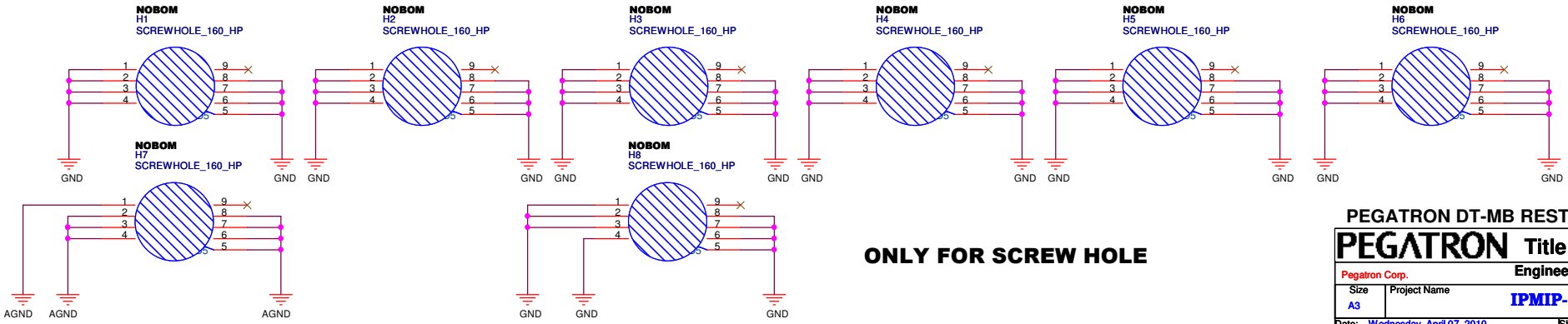
External RTC Circuitry



	ME DATA
1-2	CLEAR
2-3	Default

CLEAR CMOS & PASSWORD

CLEAR PASSWORD & CMOS		
	Clear PW	Clear CMOS
DEFAULT	3 - 5	4 - 6
CLEAR	1 - 3	2 - 4

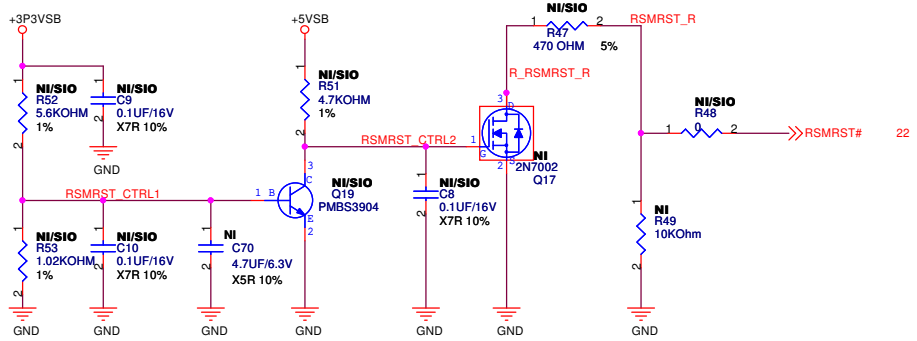


ONLY FOR SCREW HOLE

PEGATRON DT-MB RESTRICTED SECRET

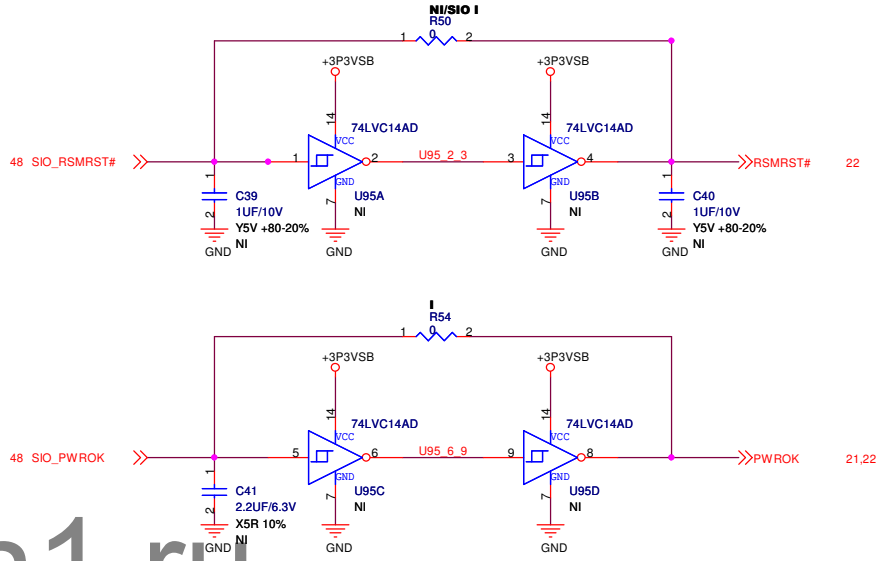
PEGATRON	Title : RTC / CMOS / KBMS	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 53 of 68	

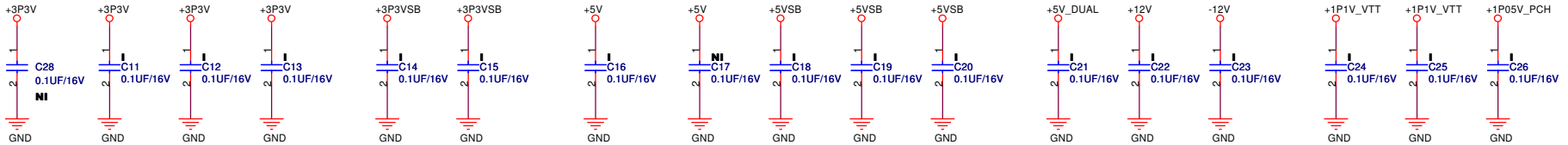
RSMRST CIRCUIT

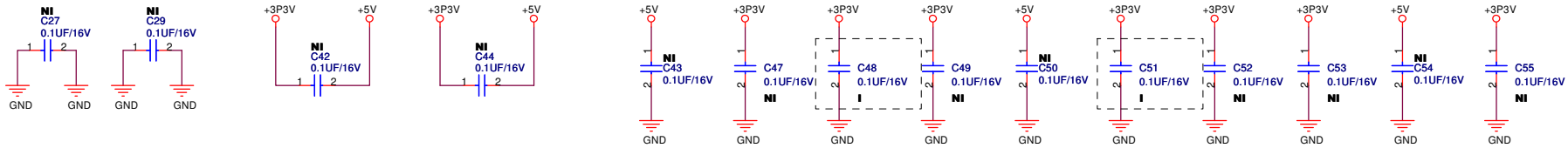


10/02/01 Modify
1.Q17,3904 to 2N7002 (0201change)
2.R52,pull high form +5VSB to +3P3VSB
3.R51,pull high from +3P3VSB to +5VSB
4.Add,C70

Schmitt-trigger for RTC issue







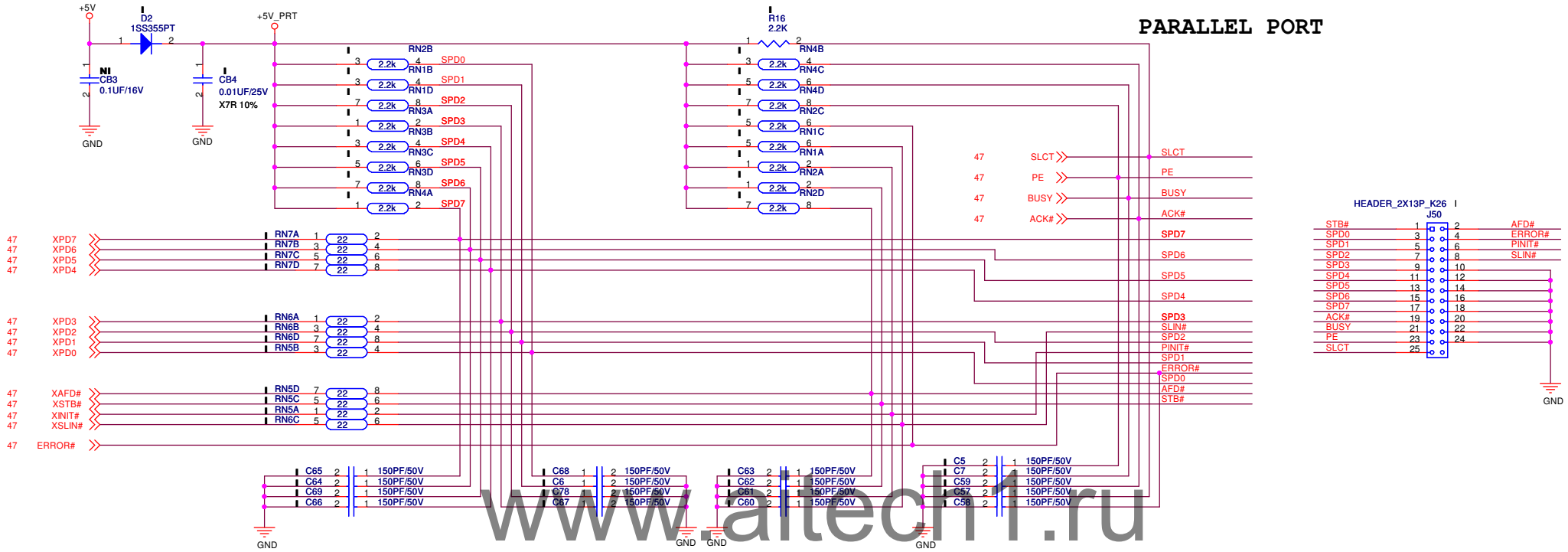
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : RSMRST CIRCUIT

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 54 of 68



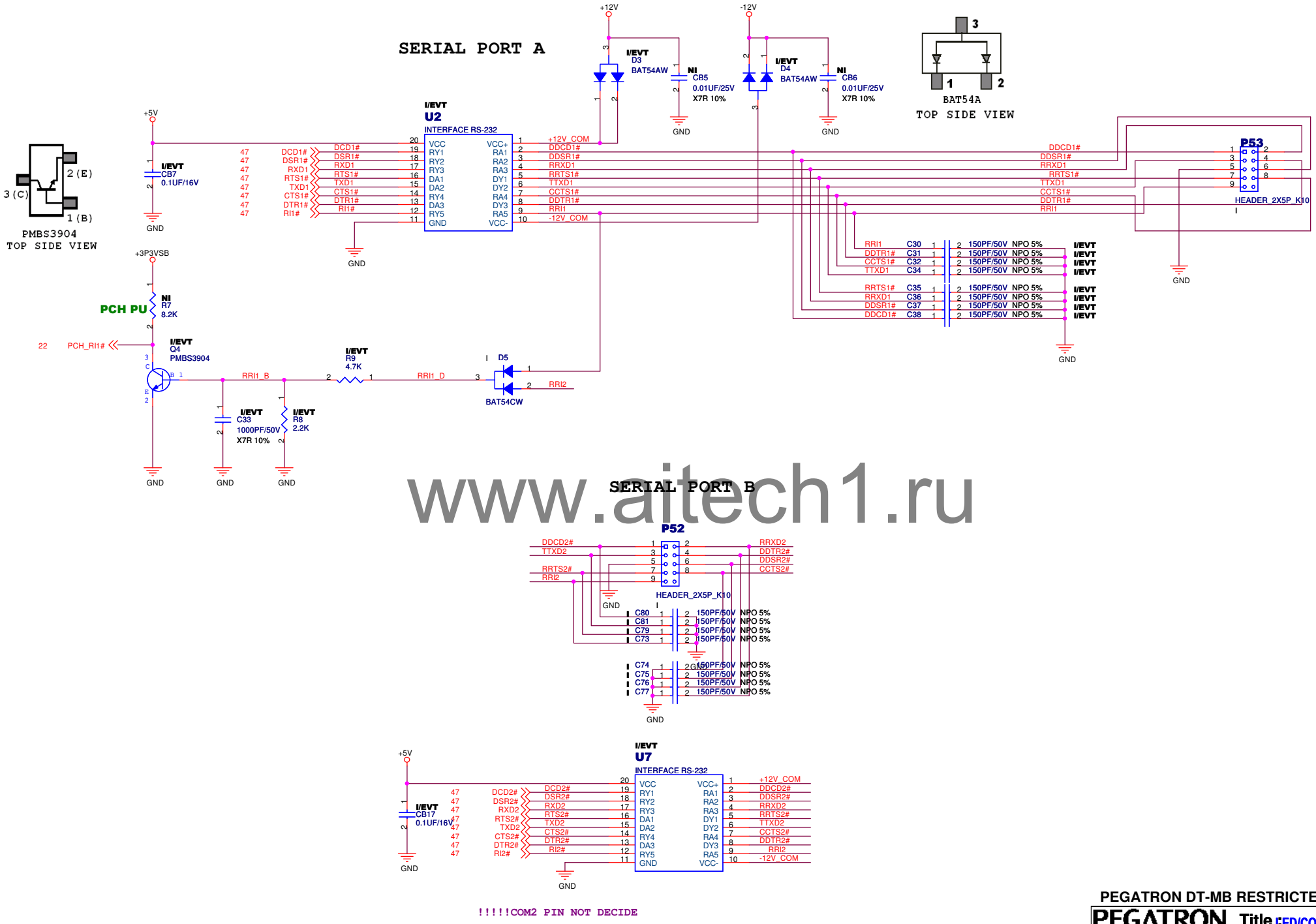
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : HDMI Connector

Pegatron Corp. Engineer: Vic_Chen

Size	Project Name	Rev
A3	IPMIP-DP	1.01

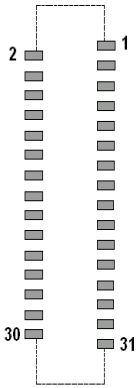
Date: Wednesday, April 07, 2010 Sheet 55 of 68



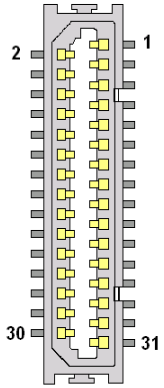
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title: LED/COM/SPKR/INTRU	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 56 of 68	

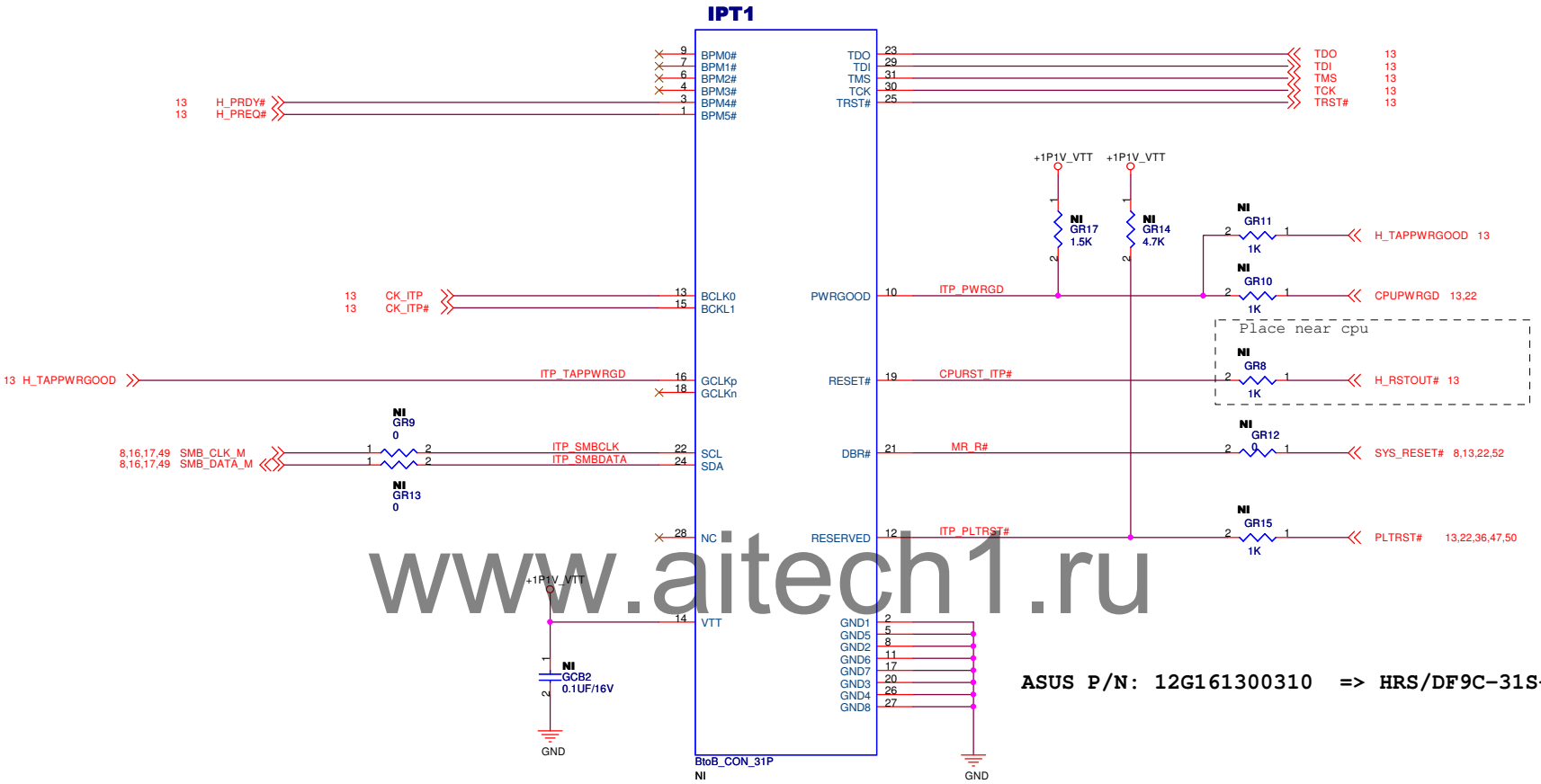
INTEL LGA-775 PROCESSOR ITP DEBUG PORT



HRS/DF9C-31S-1V(22)
PCB FOOTPRINT



HRS/DF9C-31S-1V(22)
TOP SIDE VIEW



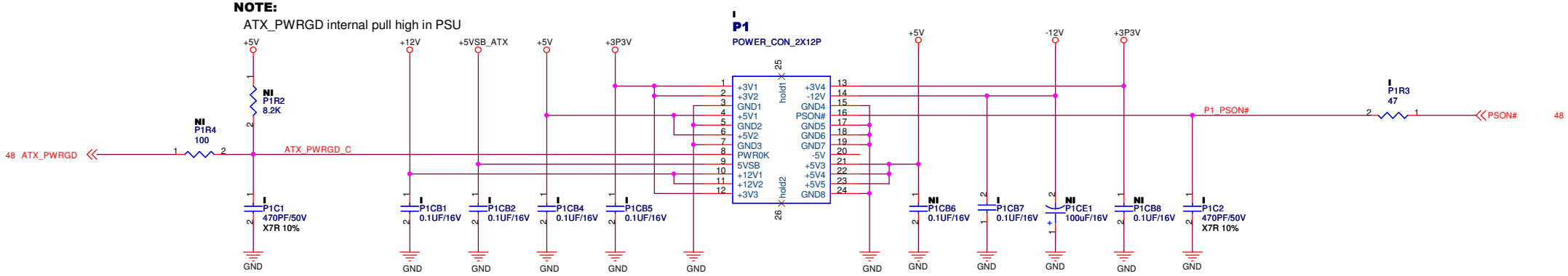
ASUS P/N: 12G161300310 => HRS/DF9C-31S-1V(22)

PEGATRON DT-MB RESTRICTED SECRET

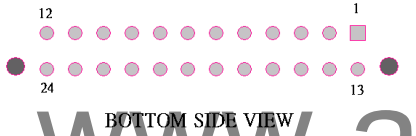
PEGATRON	Title : CPU ITP Debug CONN	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 57 of 68	

ATX POWER_24P SUPPLY CONNECTOR

NOTE:
ATX_PWRGD internal pull high in PSU



All of the Caps Around the ATX Power Connector



BOTTOM SIDE VIEW

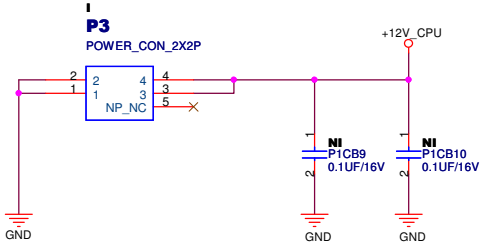
TOP SIDE VIEW

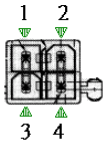
PCB

PCB38

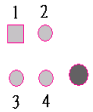
IPMIP-GS R1.00 RED
08M1-0UX0200

VRM POWER_4P SUPPLY CONNECTOR





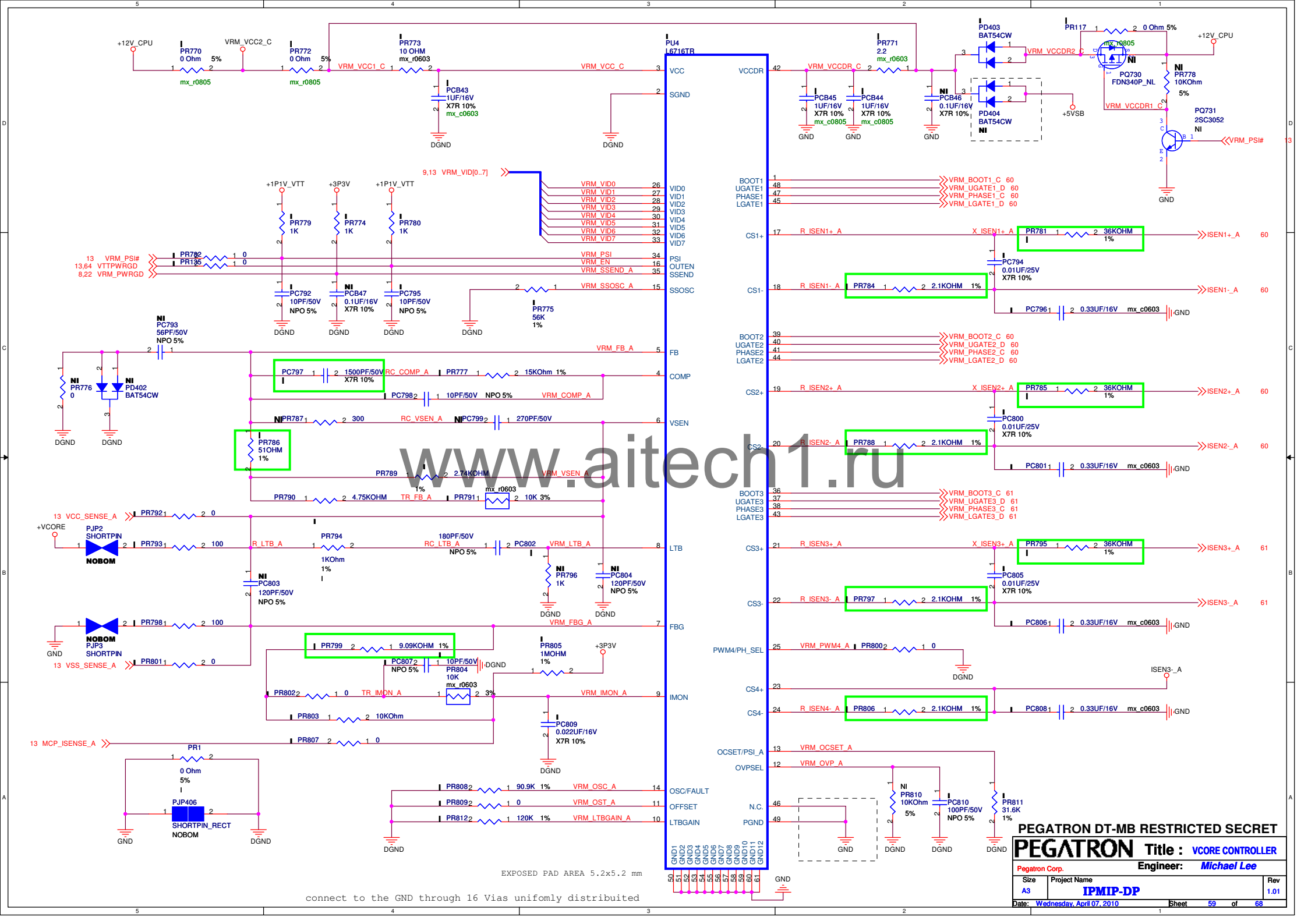
TOP SIDE VIEW



BOTTOM SIDE VIEW

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : ATX POWER	
Pegatron Corp.	Engineer: Vic_Chen	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 58 of 68	



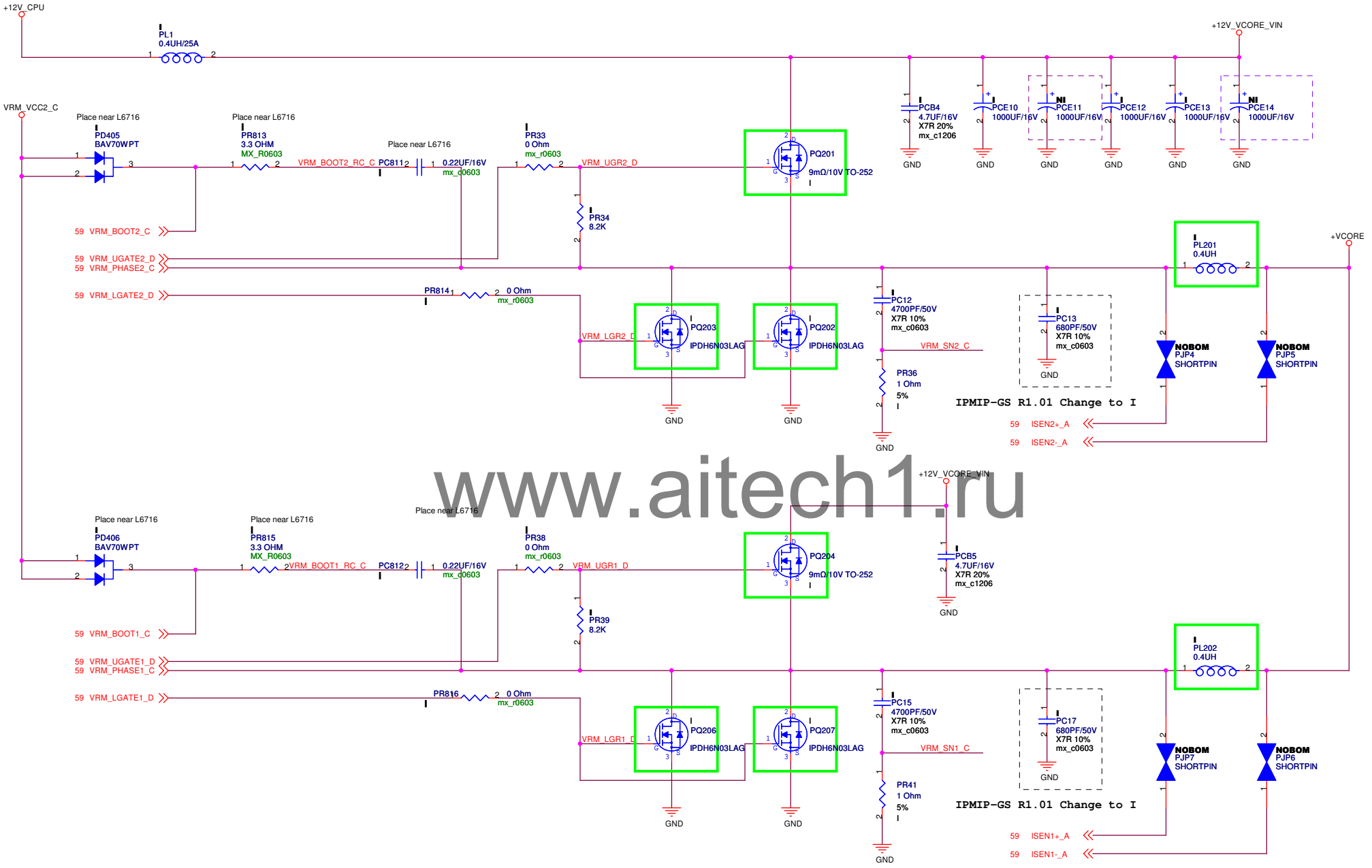
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VCORE CONTROLLER

Pegatron Corp. Engineer: Michael Lee

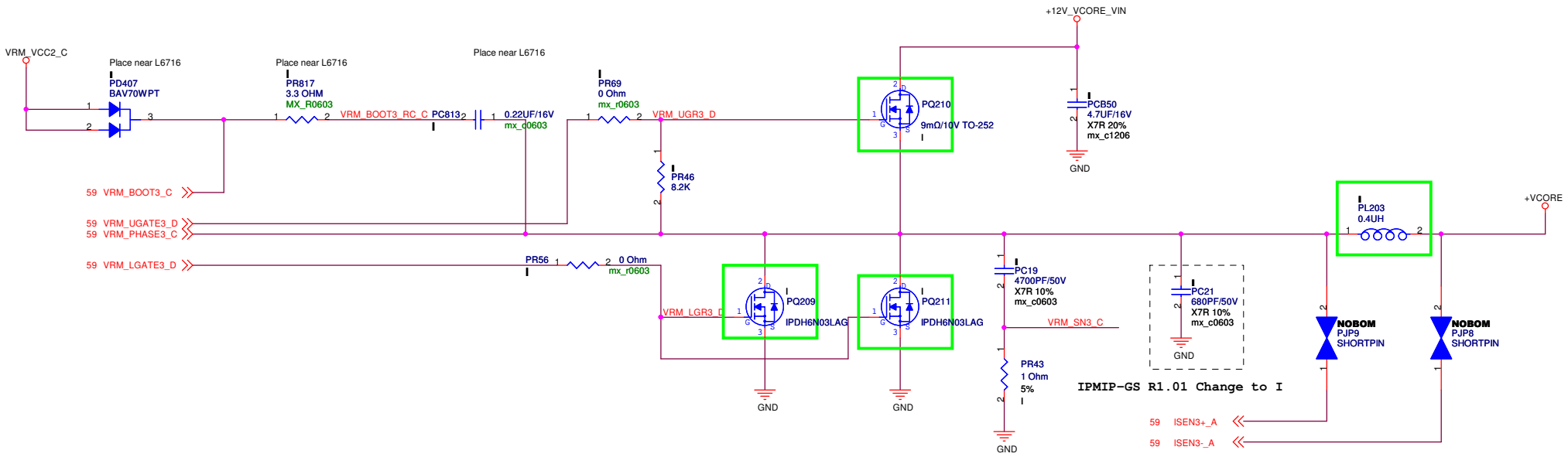
Size	Project Name	Rev
A3	IPMIP-DP	1.01

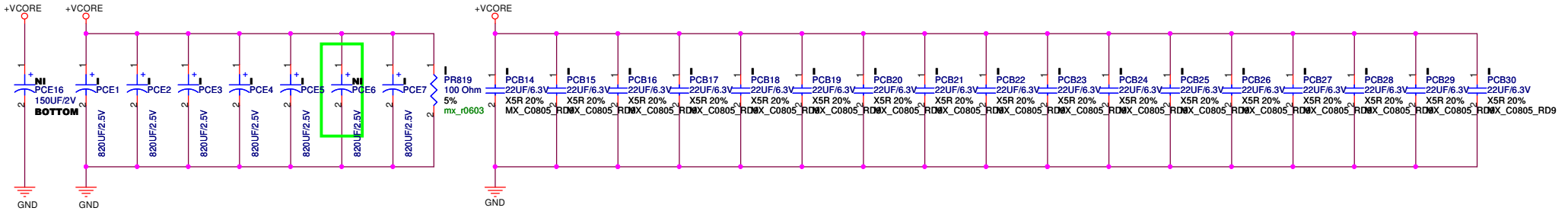
Date: Wednesday, April 07, 2010 Sheet 59 of 68



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : VCORE DRIVER-1	
Pegatron Corp.	Engineer: Michael Lee	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 60 of 68	

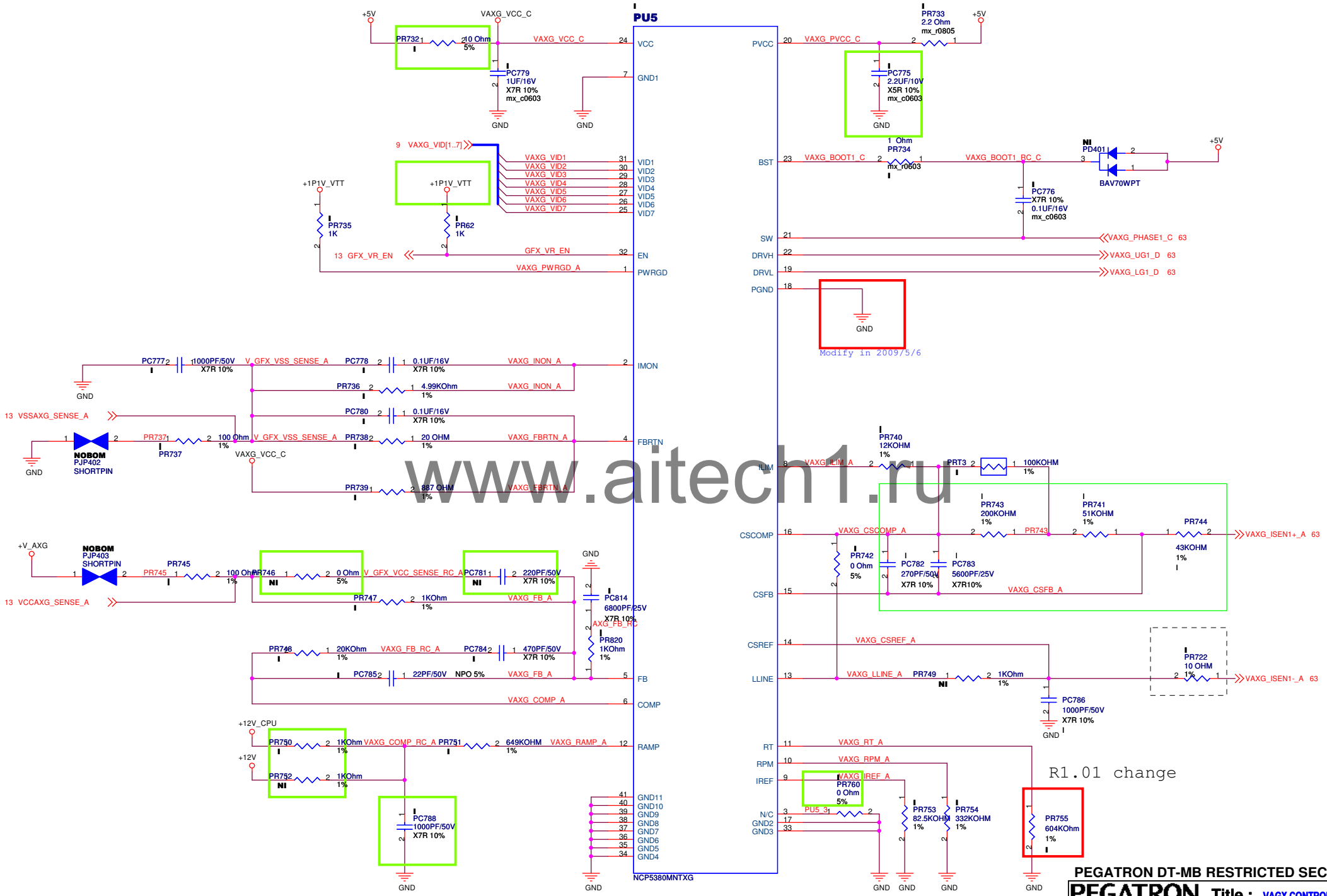




+CPU VCORE OUTPUT CAPs

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : VCORE DRIVER-2	
Pegatron Corp.	Engineer: Michael Lee	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 61 of 68	



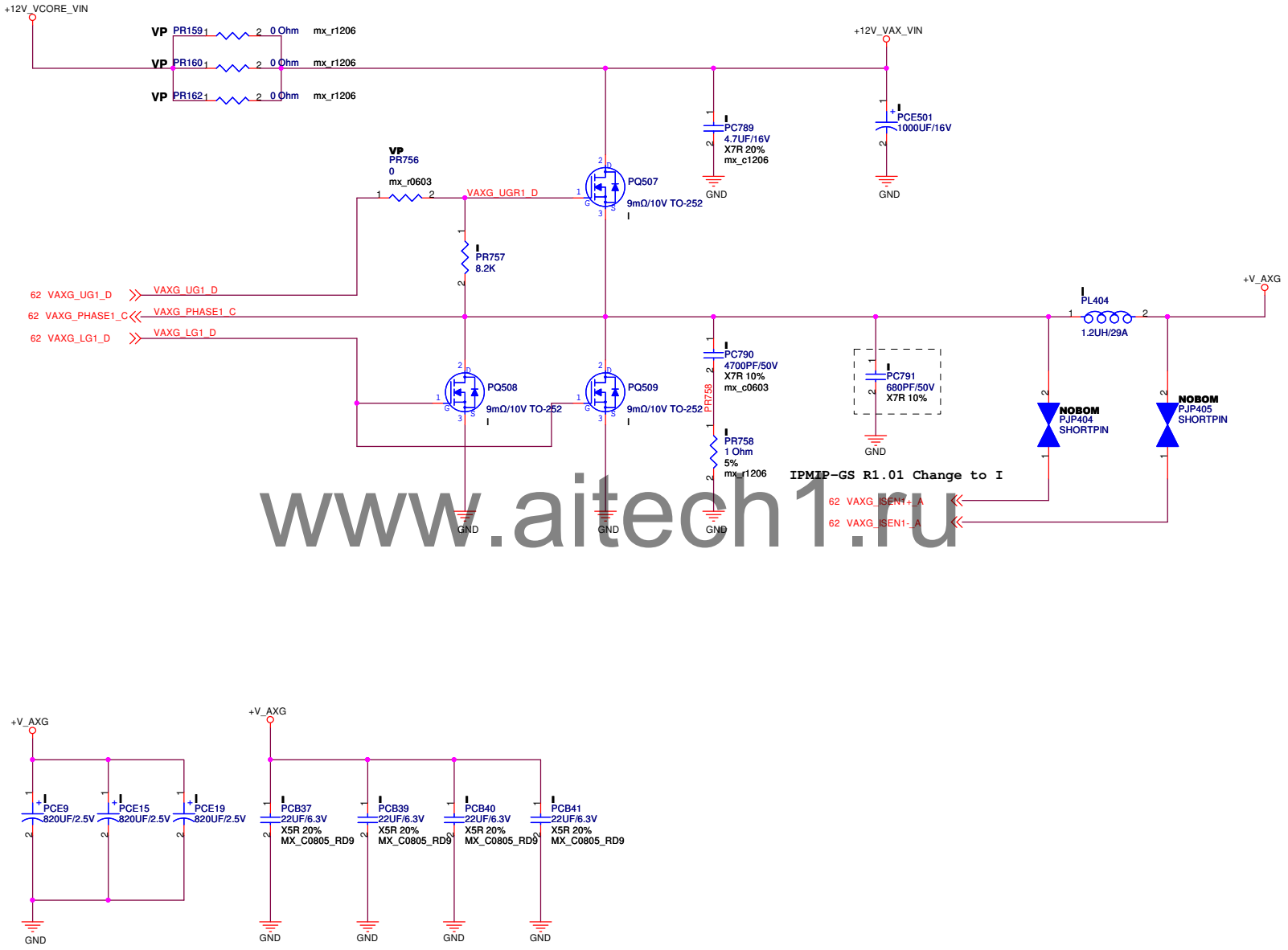
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VAGX CONTROLLER

Pegatron Corp. Engineer: Michael Lee

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 62 of 68



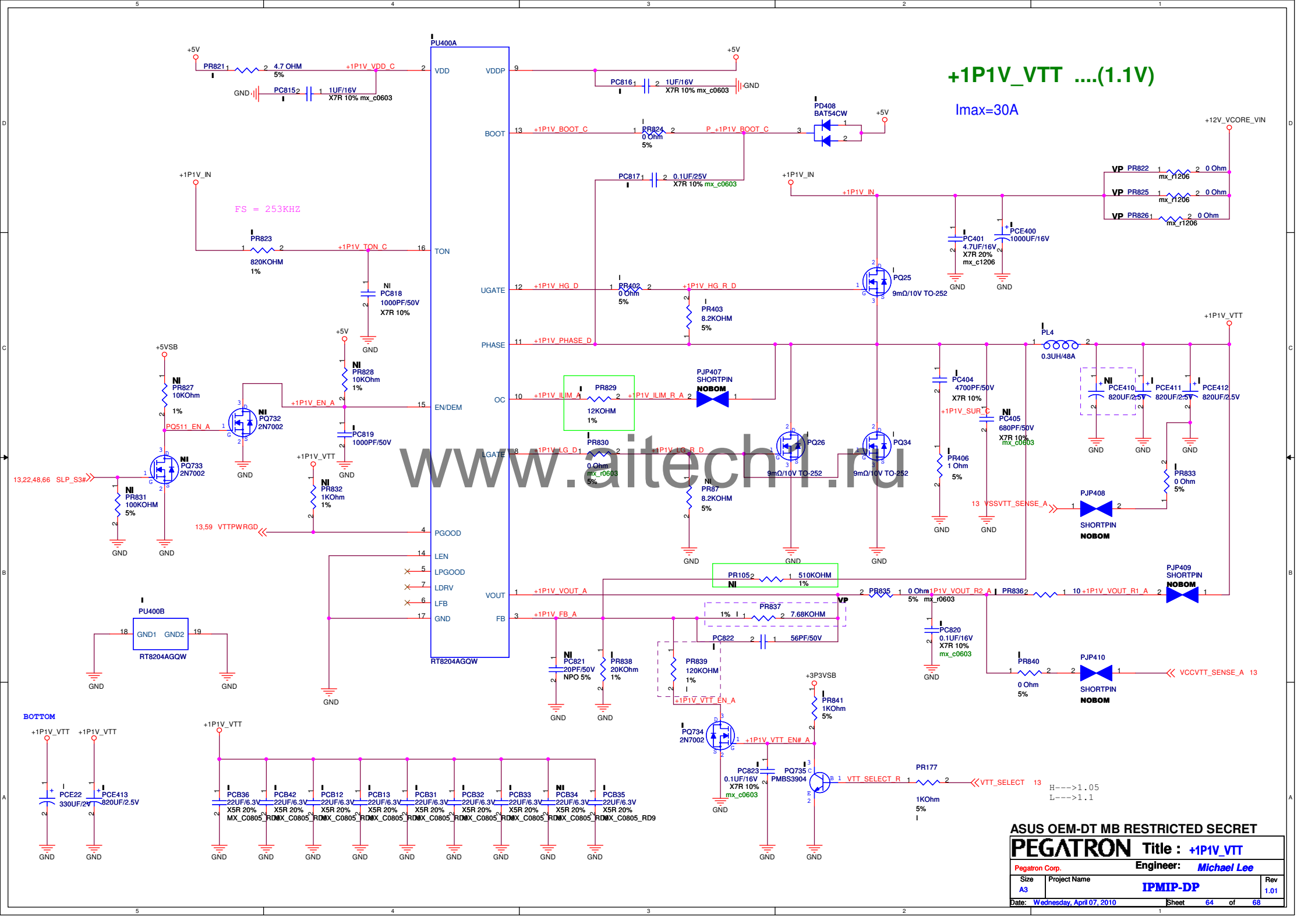
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : VAGX DRIVER

Pegatron Corp. Engineer: Michael Lee

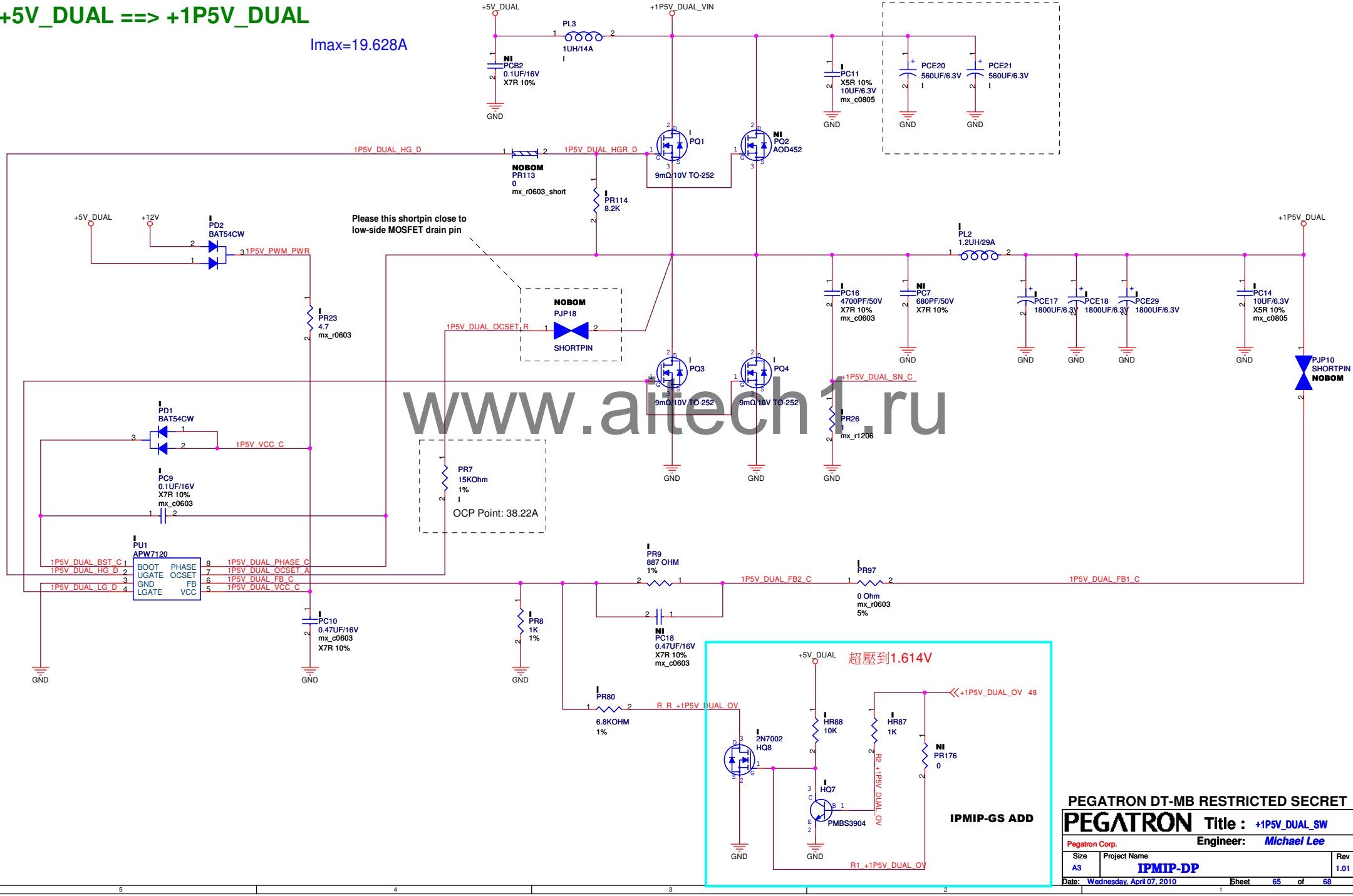
Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 63 of 68



+5V_DUAL ==> +1P5V_DUAL

Imax=19.628A



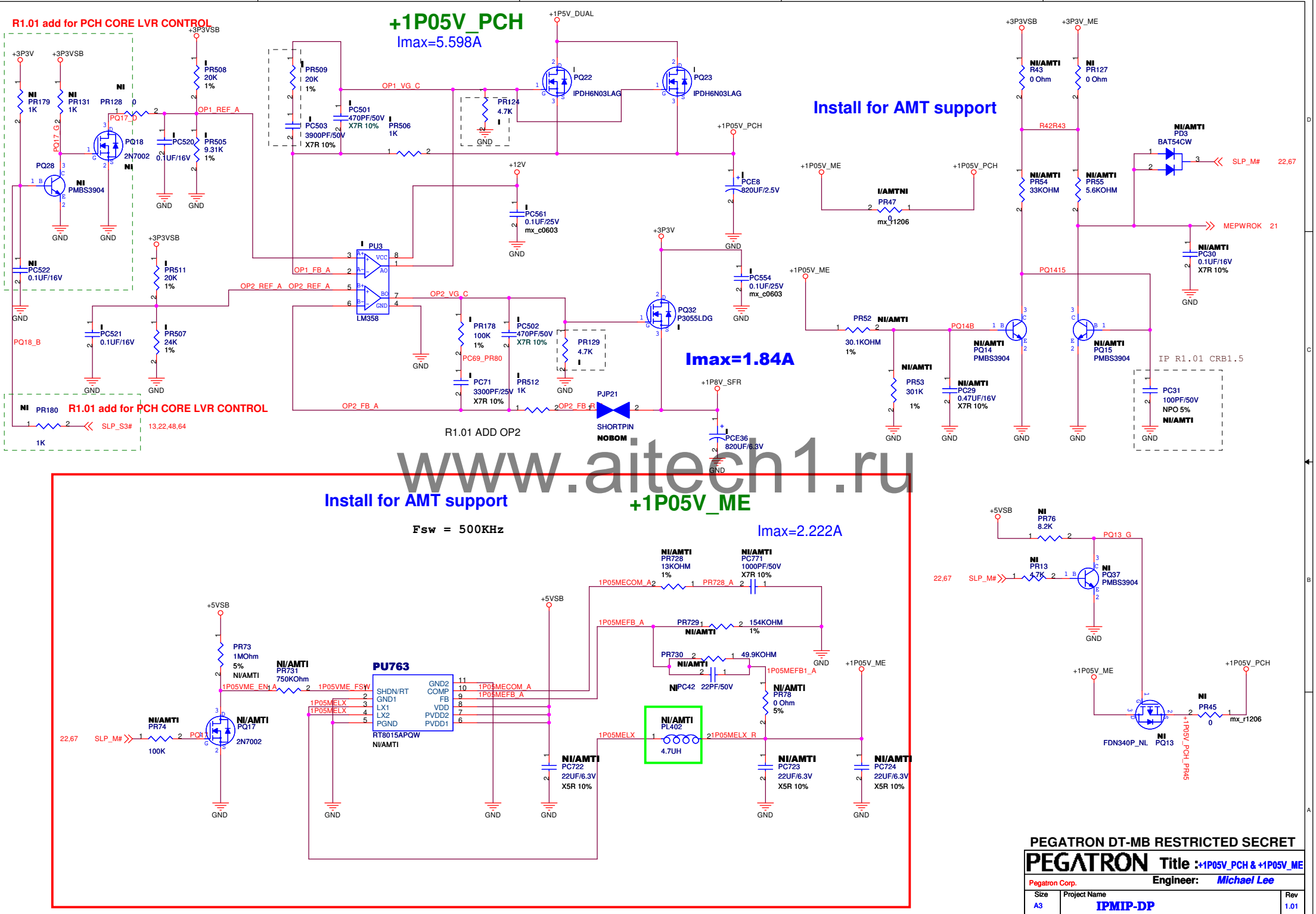
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : +1P5V_DUAL_SW

Pegatron Corp. Engineer: Michael Lee

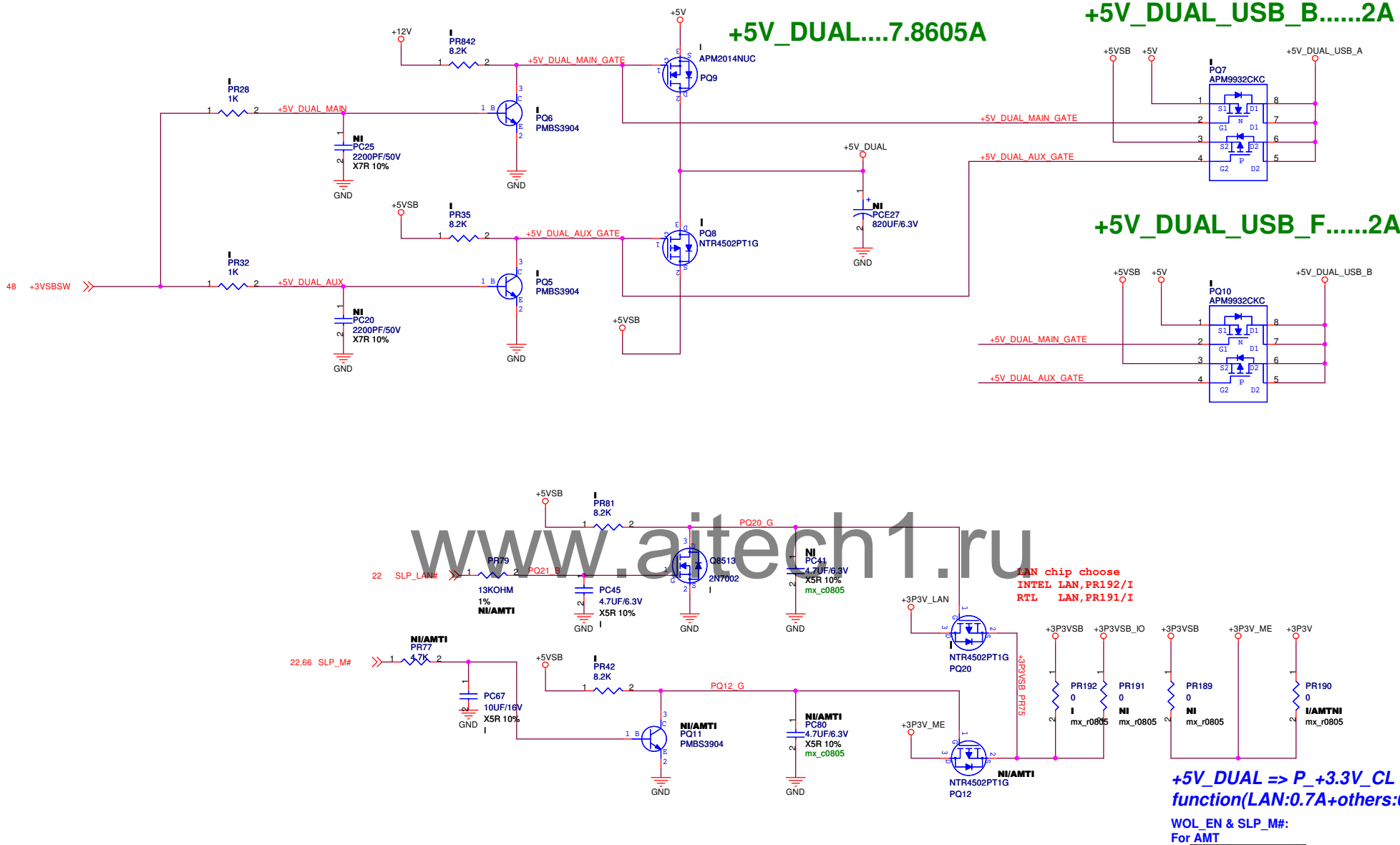
Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Wednesday, April 07, 2010 Sheet 65 of 68



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : +1P05V_PCH & +1P05V_ME	
Pegatron Corp.	Engineer: Michael Lee	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 66 of 68	

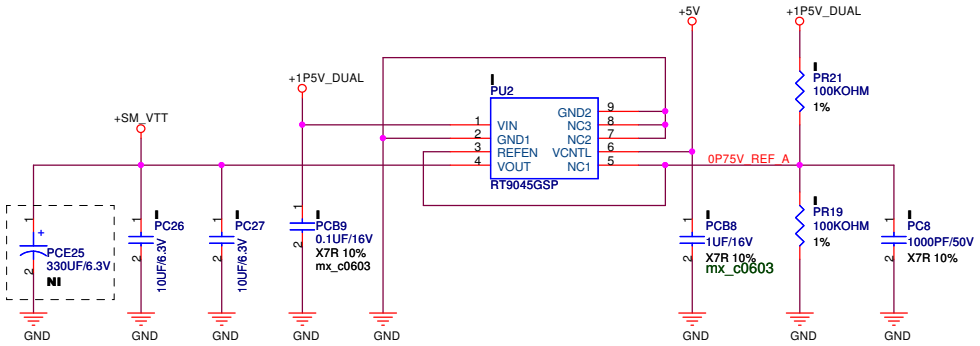


PEGATRON DT-MB RESTRICTED SECRET

PEGATRON	Title : +5V_DUAL & +3P3V_ME	
Pegatron Corp.	Engineer: Michael Lee	
Size: A3	Project Name: IPMIP-DP	Rev: 1.01
Date: Wednesday, April 07, 2010	Sheet 67 of 68	

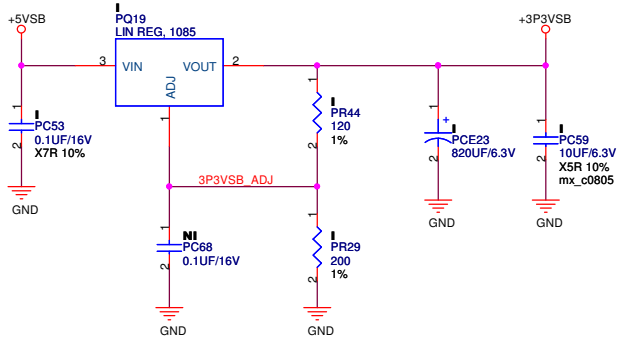
+1P5V_DUAL ==> +0P75V_VTT_DDR

Imax=0.83A



4/28 MODIFY

+5VSB ==> +3P3VSB....3.44A



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title +0P75V_VTT_ & +1P8V_SFR

Pegatron Corp. Engineer: Michael Lee

Size	Project Name	Rev
A3	IPMIP-DP	1.01

Date: Thursday, April 01, 2010 Sheet 68 of 68